Infineon Presents New Low-Power Circuit Techniques for 120-nm and 90-nm CMOS Technologies with Reduced Leakage

February 9 2005

At the IEEE International Solid State Circuits Conference 2005 in San Francisco (February 6 - 10, 2005), Infineon Technologies AG (FSE/NYSE: IFX) presents novel circuit techniques for leakage current reduction in 120nm and 90nm CMOS technologies. Scientists and Infineon's Communication business unit working in close collaboration with the Technical University of Munich have developed innovative circuit concepts to reduce leakage currents by up to three orders of magnitude. In a further research project, in cooperation with the Christian Albrechts University of Kiel, different circuit techniques were implemented, offering an optimized combination of high speed and low power consumption.

In sub-100nm CMOS technologies, it becomes increasingly difficult to manufacture transistors that offer both high switching speeds and low leakage currents. Further reduction of the minimum feature size causes an exceptionally strong increase of static power dissipation in integrated circuits due to the higher transistor leakage currents. Throughout the industry, leakage current reduction is therefore a central issue and one of the most difficult challenges to continue miniaturization in microelectronics. A combination of innovations in technology and circuit design is the key step to reduce the overall power consumption of circuits fabricated in modern CMOS technologies even with the negative side effects of the decreasing minimum feature sizes. A highly efficient circuit technique for the suppression of leakage currents is the sleep

transistor concept. The basic idea is to disconnect circuit blocks that are temporarily not required for data processing from the supply voltage by sleep transistors with a very low leakage current. The circuit blocks are reactivated by switching on the sleep transistors shortly before new data have to be processed. The great challenge to apply the sleep transistor technique in products is the proper dimensioning (i.e. choosing the width, length, and placement) of the sleep transistors to avoid high reductions of the switching speed during active operation.

“The circuit techniques that have been developed here are particularly relevant for future mobile applications, such as baseband ICs, since they enable a longer battery life despite the fact that chip functionality and number of transistors are constantly growing,” said Dr. Roland Thewes, Senior Director at Infineon`s Corporate Research.

The research teams showed that both high processing speed and low leakage current are achievable simultaneously in two core modules for digital signal processing. A 16bit multiplier-accumulator unit, designed at the Technical University of Munich in 120nm CMOS technology, operates at a maximum clock frequency of 950MHz and has a leakage current of just 20nA in stand-by mode. New fine-grained sleep-transistor concepts are explored with the multiplier-accumulator unit presented at the ISSCC. Stephan Henzler, being responsible for the low-power project at the TU Munich, emphasized: “Since the relevance of leakage currents for circuit design is continuously increasing, sleep-transistor concepts will be applied to smaller functional blocks and power down time will be reduced.”

Several 32bit adder cores with maximum clock frequencies of 500MHz to 2.5GHz were fabricated using Infineon’s 90nm triple well CMOS technology and an advanced logic family. The leakage currents were reduced to a record low value of 10nA in stand-by mode - representing a reduction by a factor of 1,000 compared to existing circuits. Moreover,

by using body-biasing techniques the threshold voltages of transistors are adjustable to adapt the circuit to the required operating mode. This improves the switching currents in active mode and increases the maximum clock frequency by up to 30 percent.

“In particular, we were able to develop a reasonable low-power strategy by combining different technology options and dedicated circuit techniques. The second key step was the experimental verification of these techniques during an early stage of technology development by means of representative circuits,” explained Dr. Christian Pacha, project manager at Infineon Technologies Corporate Research. With regard to the recently developed 65nm CMOS technology, the researchers see further challenges in improving circuit robustness in order to reduce the impact of manufacturing and technology related parameter variations.