

New DRAM circuit design approach for gigabit-era DRAM

February 16 2005

Hitachi, Ltd., in cooperation with Elpida Memory, Inc. announced that they have developed a new methodology for memory-array design, Concordant Memory Design Using Statistical Integration, which gathers statistics on device parameters from each memory cell on the chip for an accurate distribution of memory-cell characteristics, and applies the results to the quantitative evaluation of the memory array. Technology scaling at the gigabit-era introduces large fluctuations in device parameters that seriously degrade DRAM circuit performance, and it will become increasingly difficult to design a high performance circuit using conventional design methods. The concordant technique developed provides a design guideline in achieving required levels of circuit performance and will be indispensable tool for designing high-quality gigabit-era DRAM.

From high-end servers to PCs, digital home appliances, mobile information devices, etc., DRAM is embedded in a wide range of essential information devices in our daily lives. To continue to improve these devices, it is also necessary to continue to enhance DRAM performance and lower its costs. In the past, this has been achieved by scaling-down the transistors in the DRAM to develop high-speed and low-voltage operation technology. Technology scaling at the gigabit-era, however, introduces large fluctuations in device parameters, which become the source of noise which seriously degrades the readout signal voltage, a major determinant of bit failure and circuit performance. If the noise level exceeds that of the readout signal level, bit failure occurs. Thus, in DRAM circuit design, it is crucial for designers to be able to

precisely estimate the worst-case noise levels and ensure a sufficiently high read-out signal voltages.

In conventional circuit design, a "worst-case design" scenario is employed to minimize bit failure. As various noise sources must be taken into consideration, the overall noise level of the theoretical worst-case memory cell is based on the simple combination of the worst noise sources. The memory cell is then evaluated for performance, and the circuit is re-designed to give the required performance level. As parameter fluctuations increase, however, it becomes increasingly difficult to obtain a high-performance DRAM chip with a sufficiently high readout signal voltage based on the "worst-case design" scenario. Also, the probability of the worst-case cell actually existing is excessively lower than that of the actual number of worst-case cells produced in fabricated chips. Thus a new approach to circuit design, capable of providing an accurate estimate of noise levels in an actual worst-case cell and handling the expected increase in device parameter fluctuations, was required.

In response to these issues, Hitachi and Elpida devised a new DRAM design method based on a statistical model which more accurately generates the noise distributions of device parameters. Features of the new DRAM design method are described below:

(1) Statistical modeling of memory-cell characteristics

The transistor characteristics are modeled using statistical distribution curves such as the Gaussian distribution for device and circuit parameters, and calculates the read-out signal voltage and the noise level for each cell on the chip. This method gives an accurate prediction of the actual worst-case cell in the chip. The statistical model applied, is based on actual fluctuations in the device parameters and thus, represents a highly accurate status of the actual chip.

(2) Quantitative evaluation of memory array by calculated total failed bits

Using the statistical fluctuations, total number of failed bit is calculated and the proposed technique enables us to evaluate the memory array circuit quantitatively.

A DRAM chip was designed using this new approach and the total number of failed bits were calculated, and compared with the actual number of failed bits of a DRAM chip fabricated with the same parameters. A high correlation was found between the calculated and actual number of failed bits, verifying the validity of the statistical model employed in the proposed concordant memory design approach. Further, the characteristics of a memory cell with several device parameter fluctuations can be represented. Thus, it is possible to analyze the cause of all the failed bits, and provides an effective design guideline for reducing the occurrence of failed bits.

These results were presented on the 9th February at the IEEE International Solid-State Circuits Conference (ISSCC 2005), held in San Francisco, California, U.S.A., from 6th - 10th February 2005.

Citation: New DRAM circuit design approach for gigabit-era DRAM (2005, February 16) retrieved 27 April 2024 from <https://phys.org/news/2005-02-dram-circuit-approach-gigabit-era.html>

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