2-Bit-per-Cell 256-Mbit NOR Flash Memory for 3G Mobile Phone Market

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STMicroelectronics (NYSE: STM), one of the world's largest suppliers of NOR Flash devices across a broad range of applications, today announced a 256-Mbit NOR Flash memory chip that uses a well-established 2-bit/cell architecture to provide increased memory density in a small-sized die. ST's M30L0R8000x0 is the first of a series of 2-bit/cell devices that also includes a 128-Mbit IC, with a 512-Mbit chip currently in development.

Compact multi-bit cell, high density device supports advanced features in the latest generation cell phones

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Specifically designed for high-performance code execution and data storage, the 256-Mbit Flash memory is intended particularly for the third-generation (3G) mobile phone market, where increasingly sophisticated applications and multi-function capability are demanding large amounts of memory in a small physical footprint. Two-bit/cell technology effectively allows the capacity of the silicon memory array to be doubled, leading to a significant reduction in the die size and the

package.

The M30L0R8000x0 is produced using ST's state-of-the-art 0.13-micron process technology, and uses a compact 'chip-scale' 8x10mm TFBGA (Thin, Fine-Pitch Ball Grid Array) package. It is intended for operation on a 1.8V power supply (and also available with 3V I/O) for low power consumption and compatibility with the latest mobile-phone designs. ST is a major supplier of memories, especially 1.8V NOR Flash, to the mobile phone industry, and the new chip family will complement the company's extensive offering for mobile applications.

The company is also a leading provider of MCP (Multi-Chip Package) devices, in which different memory types are integrated within a single package to improve reliability and save board space for manufacturers. The new chip is already used in this way in combination with PSRAM and LPSDRAM devices for 3G phones.

The device maintains software compatibility with earlier 1-bit/cell products, and all additional processing required by the multi-level cell technology is handled on-chip. It is configured in an asymmetrical block architecture, divided into 16-Mbit banks, with a flexible block-locking scheme; fifteen of the memory banks each contain 16 main blocks of 64K words, while a parameter bank contains 15 main blocks plus 4 parameter blocks. The Parameter Blocks are located either at the top of the memory address space (M30L0R8000T0) or at the bottom (M30L0R8000B0).

Asynchronous Page Read Mode allows a consecutive-word read access time of 20nsec, while in Synchronous Burst Read mode data is output on each clock cycle at a frequency of up to 66MHz; Burst Reads can cross bank boundaries and can be suspended and resumed. The multiple bank architecture of the M30L0R8000x0 allows Dual Operations, with Read operations possible in one bank while another is Erased or Programmed,

and no delay between read and write.

Each block can be erased separately; Erase can be suspended to allow a Program or Read operation in another block, and then resumed; Program can be suspended to allow data to be read from any memory location except for the one being programmed. Each block can be programmed and erased through more than 100,000 cycles. Buffer Enhanced Factory Programming (BEFP) provides high-speed programming at typically 10 microseconds per word, using a 9V Fast-Program supply voltage.

The memory's command set is consistent with the JEDEC Common Flash Interface (CFI), the industry-wide protocol that ensures compatibility between Flash memories. Security features include a 64-bit unique device number programmed during manufacture and a 2112-bit user programmable OTP (One-Time-Programmable) cell. To conserve power in mobile applications, the device features an Automatic Standby mode, switching to Standby when the bus is inactive during Asynchronous Read operations.

The M30L0R8000T0/B0 is available in the TFBGA88 8x10mm, 0.8mm-pitch package in volume production. The device selling price is US$10.