

Soitec, ATDF to Develop Multi-Gate Field Effect Transistors (MuGFETs) for 45-nm Technology and Beyond

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In an effort to accelerate the development of new-generation transistors, Soitec, today announced its participation as the SOI substrate supplier in a development program led by ATDF -- Advanced Technology Development Facility -- the new independent subsidiary of SEMATECH for advanced semiconductor research and development. Together with two leading semiconductor manufacturers and a number of equipment suppliers and U.S.-based universities, Soitec has been involved for over a year in this advanced R&D program at ATDF, which specializes in services involving technology development, wafer processing, and analytical and electrical testing. The ATDF development program focuses on multi-gate [field effect transistor](#) (MuGFET) technology for the 45-nm node and below. MuGFET is a generic term used to describe a variety of new, multiple-gate field effect transistors, including CMOS FinFETs (FETs with "fin-shaped" transistors) and triple-gate devices.

Throughout ATDF's MuGFET program, Soitec has already supplied its SOI engineered substrates for the verification process of a 45-nm node MuGFET test chip using 248-nm lithography, which resulted in a functional, tri-gate device. In addition, Soitec is also providing SOI substrates for the development of a working FinFET transistor processed with 193-nm lithography.

The MuGFET project is one of the emerging technology development programs that ATDF has undertaken to accelerate its customers'

development progress from research to manufacturing. This partnership was ATDF's first customer-funded development program for a SOI-based device, positioning ATDF on the fast-track to ramping up its development expertise in the SOI arena. Compared to classical CMOS devices, MuGFET is a new, non-planar CMOS transistor architecture, providing the industry with an alternative design solution for keeping pace with Moore's Law and the requirements set forth by the International Technology Roadmap for Semiconductors (ITRS 2003, Emerging Research Devices). In order to improve device performance and minimize current leakage when transistors are off, semiconductor manufacturers are beginning to examine innovative transistor structures that may come into play at technology nodes at 32 nm and below. If manufacturability is proven, MuGFETs could be introduced into manufacturing within several years, and could eventually replace conventional CMOS transistors.

This new technology development effort goes beyond bulk silicon and relies heavily on the use of high quality, very thin SOI wafers as a starting material. As part of the customer program, Soitec is chartered with providing both its advanced substrates and technical support. The company's strained SOI wafers may also be considered as another substrate for future evaluation as part of this ongoing program.

"ATDF is pleased to have Soitec as a customer for one of its MuGFET emerging technology programs. Our MuGFET program would not have been able to meet its aggressive technical milestones without significant expertise in engineered substrates," said Dave Lewis, director of technology for ATDF.

"We are very pleased to work with ATDF, and leading chip and equipment makers throughout the supply chain, to provide the industry with new solutions for future technology nodes -- 45 nm and beyond -- based on our SOI technology," noted Pascal Mauberger, chief operating

officer (COO) of Soitec. "Such collaborative efforts are becoming increasingly reliant on the use of engineered substrates due to their performance benefits over bulk silicon. This is an excellent example of how the global supply-chain needs to work together in order to sustain Moore's Law as we continue to move toward smaller device geometries."

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