National Semiconductor Introduces World's First LVDS SerDes Chipset for Very High Temperature Analog Interface Applicati

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New Chipset Serializes Data at 200-800 Mbps in Harsh Automotive and Industrial Environments

National Semiconductor Corporation announced today the addition of two new high-speed analog interface chips to its industry-leading portfolio of LVDS (low voltage differential signaling) products. The SCAN921025H serializer and SCAN921226H deserializer deliver up to 10 bits of digital data at 20 to 80 MHz over a single point-to-point differential interconnect in backplanes or cable. The SerDes (serializer/deserializer) chipset operates in harsh environments up to 125 degrees Celsius.

Harsh automotive and industrial environments require a SerDes chipset that can withstand high temperatures and noise, and includes testability for continuous, reliable operation. Example applications include high-speed data transfer in electrically noisy factories and video cameras mounted in automotive roof enclosures where high temperatures are common. To enable system testing in these environments, National has integrated BIST (built-in self-test) and JTAG into the SCAN921025H serializer and SCAN921226H deserializer.

"Features such as extended temperature and JTAG further expand our high-speed analog interface market presence in the industrial and automotive segments," said Jeff Waters, product line director for the

Communications Interface division at National. "Automotive and industrial data transfer and display applications demand robust products, and National will continue to meet those needs through innovations in ruggedness and testability."

Technical Features of the SCAN921025H and SCAN921226H SerDes Chipset

National's high-speed LVDS SCAN921025H serializer transforms a 10-bit wide parallel LVCMOS/LVTTL data bus into a single high speed serial data stream with embedded clock. The SCAN921226H receives the LVDS serial data stream and converts it back into a 10-bit wide parallel data bus plus clock.

This single serial-data path makes PCB design easier, and the reduced cable, PCB trace count, and connector size significantly reduces cost. Another system cost saving feature comes from embedding the clock in the serial data stream. This eliminates the clock-to-data and data-to-data skew problem.

Upon power-up of the serializer, the engineer can choose to activate the synchronization mode or allow the deserializer to use the lock-to-random-data feature. By using the synchronization mode, the deserializer will establish lock to a signal within specified lock times. By utilizing the lock-to-random-data feature, the receiver synchronizes automatically to raw data without system intervention, training patterns, or the need for an accurate reference clock. This feature is valuable in cable applications where there is no feedback from the receiver to transmitter boards.

The SCAN921025H serializer and SCAN921226H deserializer operate between 20 MHz and 80 MHz, delivering full data payloads from 200 Mbps to 800 Mbps.

This SerDes chipset is compliant with the IEEE 1149.1 standard for boundary scan test. IEEE 1149.1 features provide the design or test engineer access via a standard test access port (TAP) to the backplane or cable interconnects and the ability to verify differential signal integrity. The chipset also features an at-speed BIST (built-in self-test) mode which allows the data transmission path between the serializer and deserializer to be verified at-speed.