Intel Builds Static RAM on 65nm Process – Set for Production in 2005

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Intel is successfully demonstrating its next-generation 65-nanometer semiconductor process at the same time it is rolling out the industry's first high-volume 90nm production.
Intel expects to ramp its 65nm process in 2005 — once again being first in the industry to produce next-generation microprocessors.
Using this next-generation process, Intel has fabricated fully functional 4-megabit static RAMs (SRAMs) with ultra-small memory cells. Smaller cells mean that processors can have larger caches that improve performance. The SRAM cells have a solid noise margin down to 0.7 volts, which indicates very robust circuit operation.

Why SRAM?

SRAM represents the industry's standard vehicle to demonstrate new process technologies.

Intel's 65-nanometer technology packs an SRAM cell's six transistors with gates just 35nm long into an area of 0.57 square micrometers. By comparison, the most advanced transistors in production today, the Intel Pentium 4 processors, contain transistors measuring 60nm.

The process flow for this next-generation effort incorporates key elements needed for advanced microprocessors, such as strained silicon transistors [PDF 236KB] and eight layers of copper interconnects using a low-k dielectric.

Extending Moore's Law

For nearly four decades chips have tracked Moore's Law, doubling their transistor count every two years. And for over a decade, Intel has set the industry pace by being first to deliver a new process generation every 2 years.

Successfully demonstrating an ultra-dense SRAM with all four million memory cells working illustrates that Intel continues to lead the industry in keeping pace with Moore's Law. Intel has a silicon roadmap to 2011 showing a new process technology being introduced every two years. The company expects to extend that roadmap in the future.

Lithography Challenge

As devices grow smaller, the lithography challenges increase, in part because feature size decreases faster than lithography wavelength.

The 65nm logic technology is being developed at Intel's D1D, the world's most advanced 300mm wafer fab. The lithography process will use masks manufactured in Intel's state-of-the-art clean room with advanced e-beam mask writers, as well as leading-edge mask technology that includes optical proximity correction (OPC), and phase shifting.

Intel's in-house mask capabilities extend 193nm lithography tools to the 65nm generation. The company's in-house mask shop enables continued scaling by using cost-effective lithography tools to increase performance at lower costs.

Source: Intel