

TSMC Verifies Fully Functional 90 Nanometer Chips Using Immersion Lithography Tools

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Findings Suggests Immersion is Nearly Ready For Production

Taiwan Semiconductor Manufacturing Company, said that it used immersion lithography tools to produce fully functional 90nm devices. The finding was presented in a keynote speech at the Cymer Lithography Symposium in Semicon Japan on December 1, predating a similar announcement.

TSMC's circuits represent the first data that immersion-based [lithography](#) systems are nearing production-ready status.

Dr. Burn J. Lin, senior director of TSMC's micropatterning division, reported in the December keynote speech that TSMC had fabricated electrically functioning 90nm SRAM chips using a 90nm-node-capable prototype immersion scanner from ASML. The wafer batch was split at ASML for both immersion and dry exposures at critical layer before metal. After developing the resist image, the wafers were sent back to TSMC to complete the fabrication steps.

Yield, device characteristics and defect levels were comparable for both dry and wet scanners. The yield-related depth of focus of the immersion scanner is almost twice that of the dry scanner.

"While some optimization may still be in order, we have promising results pointing to immersion lithography systems and tools capable of

producing functional deep-submicron devices that will scale well below the 90nm node," said Dr. Lin. "The larger focal range is the most significant finding, because it suggests that immersion tools can safely image with better yield than previously anticipated. This finding can be extrapolated to infer even greater benefits at the 65nm node."

TSMC estimates that immersion lithography tools may be called upon for 65nm production and are the chosen candidates for 45nm production. TSMC began installing its first 65nm immersion lithography system in early November this year.

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