Development of Transistor with New Metal Gate Electrode & High-K Gate Dielectric

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NEC today announced the development of a transistor featuring a new gate stack structure using a Hf-based high-k dielectric (*1) and a metal gate electrode (*2), which simultaneously realizes significant gate leakage suppression and improvement in transistor operation speed. This newly developed gate stack boasts excellent characteristics, well satisfying the requirements of 45nm-node low power transistors, and will contribute to the development of future LSIs that can meet the needs of advanced mobile terminals and digital-consumer electronics equipment due to their ultra low power consumption.

The characteristics of this new technology are as follows:

(1) By replacing the conventional polycrystalline silicon (poly-Si) with nickel (Ni) silicide as gate-electrode material on the high-k gate dielectric, the transistor current drivability is improved by 20% while maintaining the low leakage characteristics of high-k gate dielectrics. This increase corresponds to a decrease in gate leakage to one hundredth as compared with poly-Si/high-k gates, and one hundredth thousand as compared with poly-Si/SiO2 gates.

(2) The development of novel composition-controlled Ni-silicide gate-electrode technology, which is pertinent to the combination with Hf-based High-K gate dielectrics, realized a wide range of threshold voltage (Vth) control by varying the alloy composition of Ni silicide based on a simple production process. This technique enables optimum switching characteristics for both PMOS and NMOS transistors.

(3) Excellent transistor characteristics, such as sub-threshold current, carrier mobilities, and low gate leakage have been achieved. In addition, the performance of NEC's gate stack structure ensures its feasibility of up to 45nm-node low standby power (LSTP) and low operation power (LOP) transistors.

In recent years, the demand for LSI scaling technology to achieve higher speed and lower power devices is increasing. With this trend, the gate SiO2 layer, now typically thinned down to less than 2nm, suffers from a rapid increase in direct tunneling current, which leads to an increase in device power consumption. As a result, ways to suppress the gate leakage are being studied intensively. In 2003, NEC demonstrated the operation of CMOS circuits with HfSiON as a high-k gate dielectric in addition to establishing reliability technologies for it.

However, with further improvement in operation speed and consumption power in advanced LSIs, degradation of current drivability due to poly-Si gate depletion is becoming a progressively serious issue. Now, the use of metal gate electrodes in place of poly-Si is being considered as a promising solution to this issue and intensive development in this area of research is now under way worldwide. However, the following challenges have been noted:

CMOS transistors with the conventional fully silicided gate [*3] cannot obtain high drain current because their Vth's are higher for both PMOS and NMOS than the required values, despite enjoying a simple and easy production process.

Even though a suitable Vth can be obtained for PMOS and NMOS by using different metal materials, respectively, the fabrication process as well as the device structure turns out to be very complex and thus costly.

NEC and NEC Electronics have also been researching and developing

metal gate electrodes to apply onto high-k gate dielectrics for future advanced LSIs. Their newly developed gate stack structure using Ni silicide metal gate and HfSiON gate dielectrics achieves elimination of gate depletion and leads to notable improvement in both gate-leakage and transistor operation speed. Furthermore, while based on the simple production process of full silicidation, a novel approach of forming the electrodes with different Ni/Si composition ratios for PMOS and NMOS, respectively, provides suitable Vth's for both types of transistors. Such gates with different compositions are easily formed by controlling the thickness of Ni films deposited prior to the full-silicidation annealing process. Therefore, this method is a simple and reliable solution for the above-mentioned dilemma.

Using this metal gate stack, both companies will work together towards supply of advanced system-on-chip (SoC) devices with low power consumption and high speed for mobile terminals and/or digital consumer electronics equipment, and contribute to the progress of a mobile networked society. NEC and NEC Electronics will continue to make advancements in this research toward the realization of future mass production of these new transistors.

This result has been presented at the 2004 IEEE International Electron Device meeting (IEDM 2004) held on December 13, 2004 in San Francisco, USA.

Notes:

(1) **High-k gate dielectric** is a gate dielectric having a larger dielectric constant than silicon dioxide (SiO2). High-k dielectrics have lower leakage current than SiO2 under the same electrical equivalent thickness because of the larger physical thickness of high-k dielectric. NEC has mainly researched and developed HfSiON as a highly reliable high-k gate dielectric.

(2) **Metal gate electrode** is a gate electrode with a metal or a compound with metallic conductivity. The current standard gate electrode is doped polycrystalline silicon (poly-Si), which is slightly depleted at its surface due to its semiconducting nature and decreases the current drivability of MOS transistors. Metal gate perfectly eliminates such depletion and therefore it is thought to be the indispensable component for advanced LSIs.

(3) **Fully silicided gate**: A method to form silicide gate electrodes. The metal layer to be silicided is first deposited on a patterned poly-Si layer and then a sintering is conducted so that the metal spices diffuse into poly-Si and react with it fully down to the gate dielectric interface. Note that this method is quite compatible to the conventional LSI process.