STMicroelectronics Unveils Advanced Non-Volatile Memory and Advanced CMOS Platform Developments

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STMicroelectronics, one of the world's leading suppliers of semiconductor devices, will participate as presenter or co-author in fifteen papers at the IEDM 2004 (International Electron Devices Meeting) Conference, which takes place during December 13-15 in San Francisco, California. Eleven papers originating from Crolles, France, cover developments in leading-edge CMOS technology, while four are devoted to advances in Non-Volatile Memory technology developed at ST's Central R&D facility in Agrate, Italy.

"Our strong presence at IEDM, with a record number of papers, not only underlines the excellence of our Crolles and Agrate centers, but also demonstrates the productivity of the long-term research partnerships we have established," said Joel Monnier, Corporate Vice President and Central R&D Director at STMicroelectronics. "In the mainstream CMOS arena, the Crolles2 Alliance and our partnerships with world-class research institutes have enabled us to become world leaders in developing and industrializing leading-edge technologies."

Ten of the CMOS technology papers cover important topics related to the 90nm, 65nm, and 45nm platform development. In addition, some of the papers describe sub-45nm technology solutions, such as: a new method (PRETCH: Poly-gate REplacement Through Contact Hole) that allows an initially fabricated polysilicon gate and/or gate oxide to be replaced by any gate stack required to achieve a desired MOSFET

optimization e.g. for low power, high speed or I/O buffer; the first capacitor-less DRAM cell for high density embedded memories demonstrated on an SOI (Silicon-on-Insulator) substrate; first functional SRAM cells with the ST innovative thin-film technology called SON (Silicon-On-Nothing); and a demonstration of the feasibility of using Atomic Layer Deposition (ALD) instead of Physical Vapor Deposition (PVD) in the formation of porous low-k dielectrics to overcome scalability issues.. In addition, a paper co-authored by ST and research partners at LAAS-CNRS, France, and the University of Hawaii reports on substantial progress in the use of polymer electronics in microwave and millimeter wave applications.

In the field of Non-Volatile Memories, ST researchers will present two papers that reflect the Company's deep understanding of Flash technology and, in particular, of the mechanisms that affect the reliability of Flash memories. One paper reviews the important advances that have been made during the past ten years in understanding and mastering degradation mechanisms, while the second paper, co-authored by research partners at Milan Polytechnic and the Italian research institute IFN-CNR, describes experimental studies that demonstrate the existence of high-energy oxide traps that contribute to the stress-induced leakage current (SILC) that affects the degradation of data retention.

Phase Change Memory (PCM) technology has emerged as a leading candidate for the next generation of non-volatile memories. PCM memories are based on so-called chalcogenide materials that can exist in either of two stable phases: a crystalline phase that exhibits low electrical resistance and an amorphous phase that exhibits high electrical resistance, with transitions between these two states being effected by means of electrical heating of the chalcogenide material. A third paper presented by ST's Central R&D facility in Agrate, co-authored by research partners at Milan Polytechnic, provides a comprehensive analysis of the programming dynamics and phase distribution in PCM

devices.

With the continual reduction of MOSFET physical dimensions, interface effects become increasingly important in determining dopant profiles and this is of particularly significant practical importance in structures, including Flash memory cell arrays, where the device active array is made of narrow silicon strips. A fourth paper presented by Agrate researchers describes experimental and simulation studies that have resulted in the development of a model for boron segregation that has been demonstrated to be an effective tool for the development of future technology generations.