

STMicroelectronics Wins the Race to Deliver First 65-nm CMOS Design Platform

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ST completes design of full-complexity 65-nm System-on-Chip technology demonstrator

Geneva, December 16, 2004 - STMicroelectronics (NYSE:STM) today announced the important milestone of delivering a 65-nm (0.065-micron) CMOS design platform, which allows its designers and customers to start developing next-generation System-on-Chip (SoC) products for low-power, wireless, networking, consumer, and high-speed applications. In addition, ST announced the completion of a design, or tape-out, of a 65-nm complex system-on-chip to fully demonstrate its advanced technology.

ST's full 65-nm library platform includes multiple process options that allow individual cells to be optimized for high performance, low power, or general purpose use. Each option shrinks 90-nm products by half while improving speed up to 30% or reducing leakage by half in operation, thereby reducing power consumption. The platform offers two standard cell libraries, optimized for performance and density, which provide a rich portfolio of more than 1,500 cells; multiple voltage I/O cells; multiple memories; and analog IP (Intellectual Property). The cells support densities of more than 800,000 gates per square millimeter and a core supply of 1.0V or 1.2V, with metal pitches of 0.20-micron and from six to ten metal routing layers.

"Being the first to deliver a 65-nm design platform validates our alliance strategy, in general, and the efforts of the Crolles2 Alliance, in

particular," said Didier Chapuis, Group Vice President, Platform Development at STMicroelectronics. "Our customers' applications will exhibit spectacular performance at affordable costs because we've overcome the challenges to delivering the 65-nm design platform."

Further extensions to the initial platform offering, including SOI (Silicon-on-Insulator) versions and high-performance integrated passive devices, are at an advanced stage of development and will be available soon.

The new 65-nm CMOS design platform takes full advantage of the multiple features and modularity of the 65-nm process technology developed by the Crolles2 Alliance of STMicroelectronics, Freescale Semiconductor, and Philips Semiconductors. Additionally, several services, developed by the Crolles2 Alliance, are available to ease access to the technology, including: fast prototype cycle time, which is down to less than one week and has been proven for 130-nm ICs; cost reduction in mask sets; and use of e-beam technology, which allows customization without the need for masks. Also, a shuttle multi-project reticle service has started for 65-nm designs.

The 65-nm design platform is fully supported by the industry's leading CAD tools from Cadence, Mentor Graphics, and Synopsys. These tools have all been developed in close cooperation with the R&D teams of the EDA partners.

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