

New SOI transistor developed beyond 65-nm technology nodes

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20% increase in speed and 1/10 power reductions by employing back-bias control

Hitachi, Ltd. announced that it has developed a new [SOI](#) (Silicon On Insulator)^{*1)} transistor which dramatically improves speed and lowers power consumption, for processes beyond 65-nm technology nodes, in conjunction with Renesas Technology Corp. The transistors fabricated on SOI layers which have aggressively scaled buried oxide layer,^{*2)} approximately 10 nm, achieved not only increase in the drive current by 20 % but also 1/10 reductions in power consumption by using wide-range back-bias control. This transistor is expected to become a fundamental CMOS device for low-power and high-performance applications beyond the 65-nm technology nodes.

The progress of system LSI performance has opened doors to increasing the functionality of cellular phones and is sustaining a rapidly expanding market. System-on-chip (SoC) performance is measured by factors such high-speed, as well as low-power consumption, which determines the battery life of cellular phones. CMOS devices, used in SoCs, have achieved these improvements by decreasing the scale of the gate-length. In 65-nm technology node, however, it will become increasingly difficult to dismiss the increases in power consumption resulting from an increase in leakage current due to short channel effect and process variations. Thus, it was necessary to develop a new transistor structure to simultaneously achieve high-speed operation and low-power consumption beyond 65-nm technology node LSIs.

In response to this challenge, Hitachi, in cooperation with Renesas Technology, designed and proposed a completely new concept SOI transistor, and confirmed its superior high-speed and low-power characteristics. Features of the technology are as below:

(1) SOI transistor using an ultra-thin buried insulating layer:

The thickness of the insulating layer of the proposed SOI transistor was aggressively thinned to about 10nm. With conventional transistors, the switching operation is carried out by applying a bias to gate electrodes formed during the semiconductor fabrication process. With the new transistors, however, as the buried insulating layer is extremely thin, when a bias is applied to the silicon substrate, the substrate acts as "a second gate". A major benefit of this is that the controllability of switching characteristics is improved.

(2) Metal-gate-electrode-structures-enabled tunable threshold voltage^{*3)} technology:

Past SOI transistors had the merit of high-speed, but this was countered by the inability to set several threshold voltages - a necessity in SoCs. The tunable threshold voltage technology for transistors was developed by a combination of metal gate and threshold voltage adjustment ion implantation into the substrate beneath the ultra-thin buried insulating layer to achieve the desired threshold voltage.

The current-voltage characteristics of the prototype transistor was measured, and a 20% increase in drive current and one order of magnitude reduction in leak current were confirmed when the back-gate bias was applied. Further, the target threshold voltage for low-power applications were achieved by employing the developed tunable

threshold voltage technology. The next step will be to further refine the technology as fundamental high-speed and low-power CMOS technology will become essential for high performance cellular phones.

These results were presented at the 2004 IEEE International Electron Devices Meeting, held in San Francisco, California, U.S.A., from 13th - 15th December 2004.

Technical Terms:

*1) SOI: Silicon-on-Insulator.

SOI is an advanced semiconductor substrate used to produce chips that deliver higher performance and use less power. SOI improves the transistors by providing an insulating layer in the silicon that isolates the transistor, allowing electrical current to flow through the circuitry more efficiently. The insulated transistor delivers higher performance and/or lower power requirements for the chip and, in turn, for the products made with the chip.

*2) Buried oxide layer:

Referred to as BOX (Buried Oxide) layer. The BOX layer is the insulating layer embedded in a substrate with SOI substrate. SiO₂ is usually used for as an insulating material. From a viewpoint of parasitic capacitance reduction, about 100-200 nm-thick-BOX layers are employed in many cases.

*3) Threshold voltage:

Threshold voltage is one of the most important CMOS device parameter. This is defined by the voltage on which drain current begins to flow through the channel of the transistor at an ON state. At the usual bulk CMOS, this voltage is controlled by introduction of the impurities into a silicon substrate. However, SOI transistors have poor threshold voltage

controllability because the impurity concentration which can be introduced for the case of SOI transistor is limited due to formed thin SOI layer.

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