

# Silterra demonstrates functional 0.13-micron SRAM

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## *Working 8-megabit SRAM results from successful JDP with IMEC*

The Joint Development Project (JDP) between Silterra Malaysia Sdn. Bhd. and IMEC, Europe's leading independent nanoelectronics research center, has already resulted in functional SRAM chips at Silterra's wafer fabrication facility in Malaysia. The device, an 8-megabit SRAM, was fabricated in the all-copper, foundry compatible 0.13-micron CMOS process technology jointly developed by both companies.

"We are thrilled that the device works so well on the very first 0.13-micron wafer we ran in our fab," said Bruce Gray, president and interim CEO of Silterra. "The project is right on schedule with this demonstration of the phenomenal capabilities of both companies. We are now fine tuning the process, putting the customer design kit together, and we should be ready to start production in 2005 as planned."

A team of Silterra and IMEC engineers has worked diligently since the JDP was launched in July of this year. Two SRAM chips, an 8-megabit and a smaller 4-megabit device, were both functional on the initial development lot processed in Silterra's fab in Kulim, Malaysia. The process, based on IMEC's 0.13-micron technology platform, is major foundry compatible and supports up to eight layers of copper wiring.

"The achievement of these results with Silterra in only four-and-a-half months is simply amazing," stated Prof. Gilbert Declerck, president and CEO of IMEC. "I am very proud of the team's flawless execution,

dedication and commitment to the project. The success highlights the benefits of collaboration between IMEC and the industry."

The new technology at Silterra, named CL130G, will enable electronics companies to produce communication, computation and digital consumer products more cost effectively and with vastly more functionality.

Silterra plans to distribute the design kit to customers in Q2 2005 and start pilot production in July.

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