Philips highlights leading consumer-oriented semiconductor R&D at IEDM 2004

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Record-breaking performance of 90-nm RF CMOS process takes advanced development to new levels

At this year's IEEE International Electron Devices Meeting (IEDM, San Francisco, USA, 13 - 15 December 2004), Philips' R&D scientists will be contributing to no less than 17 different papers on advanced semiconductor research and development. Detailing R&D carried out by Philips in collaboration with IMEC (Belgium) and the Crolles2 Alliance (a partnership between Philips, Freescale Semiconductor and STMicroelectronics) the majority of these papers cover CMOS process development at the 65-nm and 45-nm nodes, and record-breaking RF CMOS performance at the 90-nm node. The primary focus for Philips is the development of advanced CMOS processes that are compatible with the high-volume low-cost manufacturing requirements of consumer-product applications.

"There is no point in having the most advanced semiconductor processes in the world if you cannot deliver them at the price points demanded by your customers," said Fred van Roosmalen, general manager technology partnerships, Philips Semiconductors. "With our extensive heritage in consumer electronics, our own world-class research facilities and our close partnership with some of the world's other leading semiconductor companies and research institutes, we are ideally placed to continue creating silicon solutions that meet the price/performance ratios demanded by the consumer-electronics industry."

In preparation for continued process development within the Crolles2 Alliance, Philips closely collaborates with IMEC on advanced CMOS technologies. This leading-edge research collaboration on the critical challenges in CMOS scaling keeps Philips in a highly competitive position at the forefront of the semiconductor industry.

It is the success of the semiconductor industry in keeping pace with Moore's Law - the prediction that the number of transistors on a given area of silicon doubles roughly every two years - that has been responsible for driving down the cost and enhancing the performance of everyday products such as DVD players, digital cameras and mobile phones. Although migration from 90-nm to 65-nm should be possible using technology similar to today's, hitting the 45-nm and 32-nm targets on the ITRS roadmap poses considerable challenges for the semiconductor industry.

As the thickness of the transistors' gate oxide is scaled in line with their channel length, leakage currents through an oxide layer only a few atoms thick threatens to reverse the reduced power consumption normally associated with migration from one CMOS technology node to the next. In addition, the use of new materials such as high-k dielectrics to overcome gate leakage, low-k dielectrics to reduce interconnect capacitance and new metals to replace polysilicon gates considerably increases process complexity.

For semiconductor companies serving the consumer electronics industry, this makes it increasingly important that technology improvements continue to be compatible with high-volume manufacturing methods. In addition to highlighting leading research into metal and fully-silicided gate structures, a number of the IEDM papers contributed to by Philips examine ways of minimizing the impact of new materials or manufacturing steps on process complexity and cost.

Another important area where new semiconductor technologies are set to make their mark is in RF applications. At the 90-nm node, CMOS transistors have excellent RF performance, allowing them to rival silicon bipolar solutions in some areas of mobile communications and wireless networking. Philips is presenting a paper at this year's IEDM that highlights the record-breaking performance of its 90-nm RF CMOS process. It is also presenting papers on new metal-emitter SiGe:C HBTs (Heterojunction Bipolar Transistors) that will enable low-cost silicon-based transceivers for mm-Wave (> 30 GHz) wireless applications; new substrate isolation techniques to improve the RF performance of on-chip passive components; and new methods of modeling RF MOSFET devices.

A complete list of the IEDM papers to which Philips and IMEC have contributed are listed below:

Baseline CMOS related:

A 0.314 μm2 6T-SRAM Cell Build With Tall Triple-Gate Devices for 45nm Node Applications Using 0.75NA 193nm Lithography

A Capacitor-less DRAM Cell on 75nm Gate Length, 16nm Thin Fully Depleted SOI Device for High Density Embedded Memories

Work Function Tuning Through Dopant Scanning and Related Effects Ni Fully Silicided Gate for Sub-45nm Nodes CMOS

Diffusion-less Junctions and Super Halo Profiles for PMOS Transistors Formed by SPER and FUSI Gate in 45 nm Physical Gate Length Devices

"On-the-fly" Characterization of NBTI in Ultra-Thin Gate-Oxide PMOSFETs

Poly-Gate REplacement Through Contact Hole (PRETCH): A New Method for High-K/Metal Gate and Multi-Oxide Implementation on Chip

Demonstration of an Extendable and Industrial 300mm BEOL Integration for 65nm Technology Node

Integration of ALD TaN Barriers in Porous Low-k Interconnect for the 45nm Node and Beyond; Solution to Relax Electron Scattering Effect

A Conventional 45nm CMOS Node Low-Cost Platform for General Purpose and Low Power Applications

SON (Silicon-On-Nothing) Technological CMOS Platform: Highly Performant Devices and SRAM Cells

A New Dynamic Cell-Based Performance Metric for Novel CMOS Device Architectures

Gate Stack Optimization for 65nm CMOS Low Power and High Performance Platform

45nm nMOSFET with Metal Gate on Thin SiON Driving 1150 µA / µm and Off-state of 10nA / µm

Electrical Deactivation and Diffusion of Boron in Preamorphized Ultrashallow Junctions: Interstitial Transport and F Co-Implant Control

Note: the research outlined in several of the above papers was partially funded under the European Union's IST NANOCMOS project (an integrated project in the EU's Information Society Technologies priority) or as part of the MEDEA+ framework.

RF Related:

Metal Emitter SiGe:C HBTs

New Low-Cost Thermally Stable Process to Reduce Silicon Substrate Losses: A Way to Extreme Frequencies for High Volume Si Technologies

Capacitance Modeling of Laterally Non-Uniform MOS Devices