NEC Implements Leading-Edge 90nm Vector Supercomputer Chipset with Cadence Encounter

December 13 2004

Cadence Design Systems, Inc. today announced that technology giant NEC Corp. used the Cadence Encounter digital IC design platform to develop the complete 90-nanometer chipset for one of the world's fastest vector supercomputers.
With Encounter technology, NEC achieved a 2x improvement in chip performance on its most advanced, highest performance 90-nanometer vector supercomputer chipset to date. The NEC SX-8 chipset is comprised of four 90-nanometer designs, including a hierarchical 9-million instance chip that was routed flat for final engineering change order implementation and rapid design closure.

"We are extremely pleased with Encounter's ability to meet the many challenges presented by this breakthrough design," said Takeshi Nishikawa, General Manager, Computers Division, NEC Corporation. "Encounter met all of our timing and signal integrity requirements at 90-nanometers, and reduced our leakage power by 40 percent. With Encounter's efficient memory handling and high performance, we reduced our turnaround time and time-to-market by nearly 30 percent."

"We congratulate NEC on the successful launch of this record-breaking vector supercomputer architecture and are proud that Encounter is at the core of such advanced LSI design technology and methodology," said Wei-Jin Dai, platform vice president, digital IC implementation at Cadence. "Once again, a key customer has validated Encounter's

unparalleled ability to handle extremely large and complex designs at leading-edge process technologies."