

# Magma Delivers Third-Generation Routing Technology for Nanometer Designs

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Magma Design Automation Inc. today announced that NEC Electronics America, Inc. has successfully verified a multimillion-instance nanometer (nm) design using Version 4.2 of the Blast Fusion physical design system that incorporates Magma's third-generation routing technology. In this version, advanced power, global, track and single-pass routing engines have been implemented that enhance each step of the routing process to improve routing quality and manufacturability. In addition, comprehensive design-for-manufacturability capabilities have been added throughout the routing flow to enhance yield. Runtime has also been accelerated by as much as 40 percent on a single CPU and additional runtime improvements can be achieved using advanced parallel processing capabilities. NEC Electronics America's success using this new routing technology demonstrates Magma's continuing technology leadership in nanometer design solutions.

Magma's third-generation routing capabilities were key to enabling NEC Electronics America to reduce cost by minimizing the die size and number of metal layers on this multimillion-gate design. "We used Blast Fusion and its new routing technology on one of our most complex designs that the previous router had difficulty with, due to our challenging die size and metal layer requirements," said John Fallin, general manager, Design Solutions Center, NEC Electronics America. "Blast Fusion completed the routing quickly and delivered DRC-clean designs in a single pass. The new router also delivered better results in via count and wire length. We plan to use this new router on future nanometer designs."

“Routing at 130nm and below poses new challenges in manufacturability as well as timing and signal integrity closure. At the same time, design gate counts are increasing making runtime a big concern,” said Premal Buch, general manager of Magma’s Design Implementation Business Unit. “We’ve invested a significant amount of resources to develop this next-generation router because it is a critical piece of a single-pass flow. NEC Electronics America’s ability to verify its capabilities further strengthens Magma’s position as a technology leader in IC implementation technology for 90nm and below.”

## **Magma’s Third-Generation Routing Technology**

Version 4.2 of Blast Fusion includes the following advanced routing capabilities:

**Power Routing** – A new algorithm provides users with greater flexibility in pin tapping, power ring creation, via dropping and sizing between any two power wires. This allows the router to work smoothly with rectilinear floorplans/cells and allows for full DRC checking for power at the floorplanning stage.

**Global Routing** - A new congestion estimation approach is used for better correlation with the final routing, resulting in improved routability. New crosstalk-avoidance routing capabilities have been added to improve signal integrity.

**Track Routing** – Intelligent segment spreading and jogging algorithms are implemented to provide better signal integrity and ensure routability of designs.

**Single-Pass Routing** – Several key features are included to prevent DRC and signal integrity violations for 90-nm and finer process geometries. An incremental routing algorithm is used to eliminate DRC violations

more effectively; multiple routing grids support flexible layer alignment; and enhanced pin access capability and new via-to-metal spacing rules are supported. New crosstalk-avoidance routing capabilities improve signal integrity.

**DFM-Aware Routing** – The routing engine takes into account design for manufacturability (DFM) routing rules and generates a routing topology that is compliant to the requirements and uses wire yield analysis and optimization technology to enhance yield.

**Parallel Processing** – The router features new parallel processing capabilities that combine distributed processing and multi-threading to create a highly flexible parallel processing platform that also maximizes the efficiency of the hardware environment. This provides designers with a scaleable method of accelerating routing time.

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