Infineon Achieves Breakthrough in DRAM Trench Technology

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Infineon Technologies AG presented a highly manufacturable 70nm process technology for future DRAM generations that is based on deep trench (DT) cells on 300mm wafers at the 2004 IEEE International Electron Devices Meeting (IEDM) in San Francisco (December 13 - 15, 2004). Around 25 per cent of the worldwide DRAM production today is based on trench technology. In the paper, Infineon shows the full integration scheme and the major technology features which include for the first time high-k dielectric material in a trench based DRAM manufacturing process. The results of the Infineon 70nm DRAM program represent a technological breakthrough and show the scalability of trench technology.

Infineon expects to translate the technological breakthrough in 70nm process technology into an increase of the productivity of DRAM manufacturing on 300mm wafers and its DRAM output. Smaller process structures allow a reduction in the chip size by about 30 per cent and thus increase chip output per wafer. According to the latest Gartner Dataquest forecast worldwide DRAM bit demand is expected to rise with an average growth rate of 51 per cent from 2003 to 2008, targeting a vast variety of applications from computing to data storage and consumer electronics.

The 70nm trench technology demonstrated by Infineon deploys for the first time high-k dielectric material (Al2O3) in a trench capacitor. The usage of high-k material between capacitor plates enhances the capacitance significantly and thus allows the manufacturing of smaller

capacitors. In addition, a number of technological innovations were incorporated which have already been successfully deployed in fully functional memory components manufactured in 90nm trench based DRAM technology. These innovations include a new symmetrical 'checkerboard' (CKB) cell layout beneficial for lithography and high aspect ratio etch processes.

A further enhancement of the capacitance is achieved by the introduction of hemispherical silicon grains (HSG) combined with the use of a bottle-shaped trench, both increasing the surface area of the trench capacitor and thus the capacitance of the trench storage capacitor.

DRAM technology faces enormous challenges when reducing the memory cell geometries as the substrate doping level has to be increased to overcome short channel effects. On the other hand, data retention is strongly impacted by the electric field across the device junction connected to the DRAM storage capacitor. The dependence of data retention time on increasing electric field is widely reported and basically originates from increasing junction leakage with higher doping concentration. Various solutions have been proposed, including vertical access transistors in deep trench technology or recessed devices in stack capacitor technology. The basic idea behind these concepts is to increase the array transistor channel length by extending it into the silicon surface. This enables lower doping concentrations at the expense, however, of the device drive current.

Compared to other approaches, the scalability of the new DRAM cell developed by Infineon is based on a highly asymmetric, inhomogeneous doping profile along the channel. With this concept the Infineon researchers are able to further shrink the planar DRAM cell device and to maintain a significant advantage with respect to device drive current. Another key element for maintaining the DRAM data retention time is to compensate the loss of storage capacitance caused by rapid decrease

of the feature size. In deep trench technology very large aspect ratios (depth versus width of trench) of more than 70:1 are achieved which allow realisation of sufficient capacitances in spite of smaller process structures.

Infineon is currently running most of its DRAM production on 110nm process technology, based on a trench capacitor cell exhibiting the best area efficiency in the DRAM industry. This area efficiency advantage translates into comparably small die sizes and a high number of chips per processed wafer and consequently reduced production costs.

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