IMEC reports record in tall triple-gate device SRAM cell for 45nm node

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At today's IEEE International Electron Devices Meeting in San Francisco, IMEC, Europe's largest independent nanoeelctronics and nanotechnology research center, announced that it had achieved the smallest triple-gate device SRAM cell reported to date. IMEC's device is a fully working 6-transistor SRAM cell with an area of only 0.314mm^2.

The SRAM cell achieves excellent static-noise margin of 240mV at 1.0V operation and shows good functionality down to 0.4V with a symmetric butterfly curve. Further, the cell shows great potential for scaling down to the 32nm node.

Non-planar device architectures such as multigate-FETs (MuGFET) are emerging as candidates for the 45nm node and below due to their improved current density, reduced short-channel effects, and improved gate control compared to conventionally scaled transistors.

The MuGFETs implemented in the SRAM cell distinguish themselves by a tall fin of 70nm, 40nm higher than typically reported so far, resulting in an increased current density. The transistors have a physical gate length of 40nm and 35nm wide fins. A NiSi source/drain has been used to lower access resistance and a Cu/low-k (Black Diamond) metallization finishes the cell.

Mature 193nm lithography with 0.75 NA and reticle enhancement techniques (RET) allowed the patterning of fins, gates and contact holes with 150nm pitch. The cell layout has been optimized taking into

account the different reticle (phase shift mask) technologies, illumination possibilities (Quasar or Dipole) and optical proximity corrections for each critical layer. Only uni-directional patterns are used, leading to a truly lithography-friendly design.

Currently, IMEC is pursuing the development of smaller SRAM cells and advanced logic circuits. Metal gates, using standard available materials, have been implemented to allow scaling below the 45nm node. Because of their process complexity, the SRAM cell will be used as a test module in IMEC's sub-45nm CMOS research platform. This program includes advanced lithography, gate-stack technology, ultra-shallow junctions, silicides and strain, interconnect, cleaning and emerging device programs, and aims to prove the feasibility of the developed technology elements.