IBM Demonstrates Technique for Extending Chip Performance

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IBM today announced it has demonstrated a technique that triples the performance of a standard transistor used in semiconductors by a process that is compatible with conventional CMOS technology, a major step toward achieving continued performance enhancement of chips and the electronic systems that use them.
The technique involves **the creation of a layer of the element** germanium in the critical portion of the transistor through which electrical current flows, called the "channel." Germanium has long been known to have better conductivity than silicon, and the strain in the germanium layer created by IBM's process leads to even further performance gains.

The semiconductor industry has recently embraced the concept of enhancing circuit performance by boosting the transistors' current transport properties. One such example is the introduction of strained silicon, which is in production by several companies today. Strained germanium has been shown to have significantly better transport properties than silicon or strained silicon. However, until now there has not been a path to enable the combination of strained germanium with conventional circuit fabrication techniques. IBM has demonstrated methods that can selectively place the strained germanium on the selected areas of a chip using a CMOS-compatible process.

The introduction of a new material like germanium in the critical areas of the integrated circuits provides an alternative means of improving chip performance from the traditional method of simply shrinking

circuitry. This is becoming increasingly important as further miniaturization becomes more difficult and yields diminishing returns. IBM believes this new technique could help ensure continued performance improvements in chips with circuit sizes of 32 nanometers (nm) and smaller.

"System performance depends on chip performance, and that will increasingly depend on new materials and design techniques rather than simple scaling," said T.C. Chen, IBM Fellow and vice president of Science and Technology, IBM Research. "With this work we've drawn from our experience introducing technologies like silicon germanium, silicon-on-insulator and strained silicon. Our focus is on the application of that learning to develop innovative solutions for our customers."

The introduction of new materials in semiconductors can have profound effects, often creating new problems in other areas or demanding radically different manufacturing processes. What is unique about IBM's results is that the selective introduction of strained germanium only in the critical areas of the integrated circuit provides a transistor with three times the performance without affecting other devices or circuits on the same chip. This dramatically reduces the risk of introducing a new material.

Within the transistor itself, IBM's selective strained-germanium technique actually introduces other fringe benefits. For example, the integrated circuit (IC) industry is looking for solutions to replace conventional SiO_2 gate oxide using "high-K" insulators. However, introducing a new "high-K" insulator material to the existing silicon technology is found to be especially challenging; the electrical properties of the strained germanium actually provides an easier path for the introduction of "high-K" insulators.

IBM will present the findings from this work in more detail at the

upcoming International Electron Devices Meeting (IEDM) in San Francisco.

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