Freescale enables DDR-2 memory market with low-power timing solution

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Power-efficient MPC96877 PLL clock driver optimized for DDR-2 memory modules used in computing, network storage and communications

Today's memory market is advancing to the second generation of double data rate (DDR-2) SDRAM technology. To help computing, networking and communications system developers leap to the forefront of DDR-2 memory module design, Freescale Semiconductor has introduced an advanced yet cost-effective clock driver solution optimized for the power, signal and frequency requirements of DDR-2 applications.

Freescale's MPC96877 phase-locked loop (PLL) SDRAM clock driver is engineered to provide a low-power zero-delay buffer solution for DDR-2 dual in-line memory modules (DIMMs) and onboard custom memory. The device targets desktop computing, server, router, network storage, graphic card and telecom switch applications.

Freescale has been a major provider of PLL products for more than 15 years. A pioneer in clock PLLs for the networking industry, Freescale is a leading supplier of high-end PLLs for enterprise router, switch and server applications. According to the research firm Databeans, Inc., the timing device market, which includes both clock generation devices and clock drivers, is expected to reach nearly $1 billion this year.

"Freescale's new low-power clock driver product should do well in the DDR-2 marketplace," said Susie Inouye, senior industry analyst at

Databeans, Inc. “By enabling lower power dissipation at very high frequencies, the MPC96877 provides a compelling value advantage to designers of desktop computing, high-end server and networking applications.”

“The MPC96877 is designed to run cool, fast and accurately for a wide range of DDR-2 applications,” said John Fairholme, director of operations for Freescale’s Timing Solutions. “Memory module manufacturers continually seek ways to reduce power while increasing frequency. Heat also can have an adverse affect on the long-term reliability and performance of memory modules. By operating at exceptionally low power and thus enabling cooler operation, the MPC96877 provides an optimal solution for our customers’ needs.”

The power dissipation of the MPC96877 is among the lowest in the industry. The device’s application frequency scales from 160 MHz to 450 MHz.Its maximum operating frequency (fMAX) capability is 500 MHz, which exceeds the JEDEC specification and makes it the fastest DDR-2 clock offering available. In addition, the MPC96877 has a low frequency capability (fMIN) that’s significantly below the JEDEC specification, which enables customers to develop cost-effectivetest platforms with frequencies as low as 25 MHz. The MPC96877 is also designed to track spread spectrum clocking for reduced electromagnetic interference (EMI).

The MPC96877 device meets or exceeds the JESD82-8 PLL JEDEC standard for PC2-3200/4300, provides a 1-to-10 differential clock distribution, and is designed to provide best-in-class performance based on:

- Low skew, low jitter and high frequency
- Sophisticated characterization
- Exceptional signal integrity

To provide customers with a comprehensive DDR-2 memory clock driver solution, Freescale also plans to offer the MPCSSTU32864/A buffer, which works in tandem with the MPC96877. A non-parity device, the MPCSSTU32864/A is planned to be the first in a family of buffer registers that will also include a parity version. The “A” version of the device, with its 1.8 ns Tpd, is designed to meet the demands of increasingly tight timing budgets.

In addition, Freescale recently has announced a family of next-generation 90-nanometer (nm) PowerQUICC™ III communications processors containing PowerPC® cores with integrated DDR memory controllers that support DDR-2 SDRAM at up to 333 MHz (up to 667 MHz data rate, with initial offerings at 533 MHz data rate).

The MPC96877 DDR-2 memory clock is manufactured on 1.8V 180-nm low-voltage CMOS technology for low-power consumption and low-cost designs. The MPC96877 device is available in two package options: a lead-free 52-ball BGA and a lead-free 40-pin QFN. The device is designed to operate from 0degrees C to 70degrees C.

Availability

MPC96877 DDR-2 clock driver samples are available now, and production is planned for Q2 2005. MPCSSTU32864/A buffer register samples are planned to be available in Q1 2005, with production planned for Q2 2005.

Initial samples of Freescale’s 90nm PowerQUICC III processors with DDR-2 support are planned for Q2 2005.