Elpida Memory Develops 90 nm Silicon Wafer Process for High-Performance DDR2 SDRAM

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Advanced Process Technology Boosts Production Efficiency for Superior DDR2 Products

Elpida Memory, Inc., Japan's leading global supplier of Dynamic Random Access Memory (DRAM), today announced that is has developed its new 90 nm production process for high-performance DRAM products. 90 nm (or 0.09 micron) is the next-generation measurement for silicon wafer manufacturing, following 100 nm (or 0.10 micron). It will allow more silicon chips to be produced on a single wafer because the size of each chip is smaller, and it improves overall production efficiency. Elpida's 90 nm process technology will first be applied to the production of high-performance 512 Megabit and 1 Gigabit DDR2 SDRAM products starting next year.

"Each transition to a smaller process geometry is no easy task and involves development of the process, followed by development of a new device design, and finally production using the new process and design together," said Yukio Sakamoto, president of Elpida Memory, Inc. "Elpida has verified this new 90 nm process technology and demonstrated high production yields equivalent to that of our currently mass produced 100 nm-based devices. During mass production, we anticipate an increase in productivity by 20% or more from our new 90 nm production process."

Elpida's 90 nm Process Technology

Elpida is using the same KrF optical lithography - with a wavelength of 248 nm - that is used for current mass production of 100 nm devices in its new 90 nm lines. Combined with the use of Optical Proximity Correction (OPC) the new process refines and reduces the geometric size of the memory cell and its peripherals by 90% while maintaining high production yields. The defect level defining the yield in production of the new 90 nm process has been confirmed to be as low as that of Elpida's mass-produced 100 nm process.

Elpida also implements an original silicide contact technology. With the 90 nm process, the geometry of the contact hole for the connecting nodes in the circuitry also becomes smaller. Consequently, this introduces additional resistance around the circuitry and impacts the speed performance. By introducing this silicidation technology, this problem has been greatly reduced, enabling DDR2 SDRAM to achieve speed performances on the order of 667 Mbps, 800 Mbps and beyond.