Elpida Memory Develops Distortion Control Technology to Improve Mass Production of Highly-Reliable DRAM

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Elpida Memory, Inc., Japan's leading global supplier of Dynamic Random Access Memory (DRAM), today announced that it has developed a new distortion control technology that improves data retentiveness-an element that is crucial for obtaining high yields of high-performance DRAM products during the mass production phase. The technology was developed in partnership with NEC Corporation System Devices Research Laboratory. The technology also allows volume-produced DRAM to achieve the higher performance necessary for future applications while remaining cost-competitive. These achievements were presented at the 2004 International Electron Devices Meeting (IEDM) held in San Francisco on December 13-15, 2004.

Elpida plans to apply this innovative technology to all of its current and future DRAM products.

Technical Document

This document contains an overview of information that was jointly presented by Elpida Memory and NEC Corporation System Devices Research Laboratory at the 2004 International Electron Devices Meeting (IEDM) held in San Francisco on December 13-15, 2004.

Distortion Control Technology for Improved Data

Retention

Overview

Since DRAM memory cell leakage current determines data retention characteristics, identifying and controlling causes of this leakage is necessary in order to achieve high-yield mass production of high-performance DRAM. By newly ascertaining and controlling the strain mechanisms that contribute to the formation of imperfections that result in significant leakage current, Elpida and NEC Corporation System Devices Research Laboratory have established new technologies to dramatically enhance DRAM cell data retention time.

Background

In DRAM, a capacitor is connected to a memory cell transistor. An electrical charge stored in the capacitor is one bit of memory information. One of the most critical parameters of a DRAM cell is its data retention time. Due to leakage current the capacitor discharges gradually, so all of the cells in the memory need to be refreshed (recharged) periodically, at intervals depending on the configuration and operating parameters of the device. Between refresh cycles each cell must retain its charge for a minimum time. If the charge stored in the capacitor "leaks out" to another location, then a failure in data retention occurs. With advancements in the miniaturization of device elements, the surface areas of memory cells are rapidly becoming smaller and thus it becomes more difficult to ensure a sufficient amount of stored charge for data retention.

Purpose and Focus

Identifying the factors that degrade data retention characteristics is

crucial. It has been evident that there are electrical leakage factors that directly degrade data retention. It has now also become clear that associated with degradation of data retention time there are microscopic crystallization imperfections about 10 nm (nanometers) in size that are present in cell transistors. According to crystallization analysis, the imperfections that degrade data retention characteristics occur during cell transistor production, forming in areas where there is localized distortion in the cell transistors due to stresses introduced during manufacturing steps. The strain mechanisms that generate the crystallization imperfections were then identified by reviewing several hundred existing DRAM manufacturing processes capable of generating the various stresses that result in the distortions. Similarly, researchers also isolated point defects, instances of process artifacts and material impurities that cause the excessive concentration of certain structural distortions in regions of the cell transistor, in turn contributing to degradation of data retention time. The team determined that stress mechanisms also impact the formation of these defects, and was able to determine stress conditions under which the defect growth can be stabilized.

By studying the combined effects of carefully controlled annealing (heat treatment) at several stages of manufacturing, the researchers developed a technology model to control the various stresses, or strain mechanisms, contributing to both crystallization imperfections and point defect growth that are related to leakage current. This technique, referred to as "lattice strain design," can be applied in production to greatly increase the data retention time of DRAM.

Achievements

These two breakthroughs allowed the experimenters to develop technologies for the optimization of cell transistors by the use of a new heat treatment process that carefully controls the internal stresses arising

in materials during DRAM manufacturing. As a result, the leakage current that stems from crystallization imperfections and point defects is reduced and data retention characteristics are improved two fold over the characteristics of conventional DRAM.

In future high-performance DRAM products, we anticipate that the introduction of new materials and further miniaturization of cell transistors will make distortion control technology an indispensable capability. Elpida plans to apply this innovative lattice strain design technology to all of its current and future DRAM products.