

AMD, IBM announce breakthrough strained silicon transistor

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[AMD](#) and [IBM](#) today announced that they have developed a new and unique strained silicon transistor technology aimed at improving processor performance and power efficiency. The breakthrough process results in up to a 24 percent transistor speed increase, at the same power levels, compared to similar transistors produced without the technology.

Strained silicon technology:

Strained silicon increases transistor drive current which improves switching speed by making current flow more smoothly. Strained silicon is a process to raise drive current in both types of CMOS transistors. Using a very thin layer of single-crystal silicon with built in stress, or strain, improves drive current, making the devices run faster. At the molecular level, this silicon resembles a lattice. Stressing, stretching, or straining, this lattice lets electrons flow with less resistance. Lower resistance means that transistors switch states faster and that makes chips compute quicker. Drive current measures the amount of current flowing from source to drain in the transistor. Higher drive current causes a transistor to switch between its on-off states faster, ultimately creating a higher frequency. This gives a substantial gain over the existing 0.13 micron processes while only increasing the manufacturing cost by two percent.

Faster, more power-efficient transistors are the building blocks of higher performance, lower power processors. As transistors get smaller, they operate faster, but also risk operating at higher power and heat levels due to electrical leakage or inefficient switching. AMD and IBM's jointly developed strained silicon helps overcome these challenges. In addition,

this process makes AMD and IBM the first companies to introduce strained silicon that works with silicon-on-insulator (SOI) technology, resulting in an additive performance and power savings benefit.

“Innovative process technologies such as strained silicon enable AMD to deliver more value to our customers,” said Dirk Meyer, executive vice president, Computation Products Group, AMD. “Our shared progress in developing advanced silicon technologies allows AMD to deliver today’s best performance per watt, and this strained silicon development is expected to extend that leadership when we begin shipping the dual-core AMD Opteron™ processor in mid-2005.”

AMD intends to gradually integrate the new strained silicon technology into all of its 90nm processor platforms, including its future multi-core AMD64 processors. AMD plans to ship the first 90nm AMD64 processors using the technology in the first half of 2005.

IBM plans to introduce the technology on multiple 90nm processor platforms, including its Power Architecture-based chips, with the first products slated to begin shipping in the first half of 2005.

“Innovation has surpassed scaling as the primary driver of semiconductor technology performance improvements,” said Lisa Su, vice president of technology development and alliances, IBM Systems & Technology Group. “This achievement with AMD demonstrates that companies willing to share their expertise and skills can find new ways to overcome roadblocks and help lead the industry to the next generation of technology advancements.”

The new strained silicon process, called “Dual Stress Liner,” enhances the performance of both types of semiconductor transistors, called n-channel and p-channel transistors, by stretching silicon atoms in one transistor and compressing them in the other. The dual stress liner

technique works without the introduction of challenging, costly new production techniques, allowing for its rapid integration into volume manufacturing using standard tools and materials.

AMD and IBM researchers are the first in the industry to simultaneously enhance the performance of both types of transistors in a semiconductor using conventional materials.

“This breakthrough in strained silicon engineering is a result of our joint development alliance and the efforts of our partnered teams at IBM’s facility in New York and AMD’s facility in Germany,” said Nick Kepler, vice president of logic technology development, AMD. “This is a better way to deliver the performance enhancements and power reduction that AMD Opteron™ and AMD Athlon™ 64 processor customers expect.”

Details of the AMD-IBM Dual Stress Liner innovation will be disclosed at the 2004 IEEE International Electron Devices Meeting in San Francisco, Calif. from December 13-15, 2004. The Dual Stress Liner with SOI technology was developed by engineers from IBM, AMD, Sony and Toshiba at IBM’s Semiconductor Research and Development Center (SRDC) in East Fishkill, NY, as well as engineers from AMD at its Fab 30 facility in Dresden, Germany.

IBM and AMD have been collaborating on the development of next-generation semiconductor manufacturing technologies since January 2003.

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