Artisan and Cadence Collaborate to Optimize Low-Power Chip Design

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New Library Views Support Next-Generation Low Power Devices

Artisan Components and Cadence Design Systems, Inc. today announced their collaboration to provide library views that enable designers to more effectively **optimize low-power** chip **designs**. The companies have partnered to create and qualify Artisan library views based on the Cadence® effective current source model (ECSM) format. These views provide customers with accurate delay prediction across a wide range of voltage levels and operating conditions using the Cadence Encounter™ digital IC design platform.

To meet the increased challenges of lower-power designs, customers are adopting methodologies that vary the supply voltage to enable a more effective trade-off between performance and power. These methods require additional timing views to predict chip performance at different voltage levels. The different voltage levels may be intentional variations for power savings or the result of IR drop and ground bounce. ECSM is a revolutionary new modeling format that enables designers to accurately predict timing under any combination of voltage conditions.

"We were able to model IR drop impact on delay using the Cadence Encounter delay calculator with Artisan's ECSM (lib_ecsm) library views for extended voltage range on our recent 130-nanometer production design," said Li-Siang Lee, Physical Design Manager, Cortina Design Systems. "This allows us to model, prior to tape-out, effects that previously were observed only in silicon."

To achieve and verify the necessary accuracy levels for the ECSM (lib_ecsm) delay models at different voltage levels, Artisan and Cadence performed qualifications using Artisan's SAGE-X™ standard cell library and measured delays against SPICE while varying voltage, slew and load. The average difference in measured delays between SPICE and ECSM was 0.5%.

"Artisan realizes that a single company cannot address today's power consumption challenges alone and it takes collaboration among leading companies to help customers achieve faster time to market with first-pass silicon," said Neal Carney, vice president of marketing at Artisan. "Our collaboration with Cadence allows us to provide library views that enable balancing power reduction techniques with high-performance design specifications to meet customers' nanometer requirements."

"With the growth of today's semiconductor industry being driven primarily by the wireless and digital consumer markets, the impact of power consumption in these devices is a significant issue for designers," said Jan Willis, senior vice president of industry marketing at Cadence. "Our collaboration with Artisan provides critical low power design chain capabilities to uniquely address the challenges of next-generation semiconductor technology."

Availability
ECSM models (lib_ecsm) that support extended voltage range for Artisan's SAGE-X, SAGE-HS and Metro standard cell libraries at 130nm and 90nm processes are available upon request.