Xilinx Delivers Breakthrough Design Tool For High Performance Signal Processing With New System Generator For DSP v6.3I

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New tool dramatically accelerates productivity and closes the DSP design gap by combining the benefits of C-based and HDL flows within a single solution

Xilinx, Inc. today announced it's next generation System Generator for DSP v6.3i development tool with full support for the company's flagship Virtex-4 Platform FPGAs. Furthering Xilinx's XtremeDSP initiative, System Generator v6.3i provides enhancements that make it easier for designers to build high performance digital signal processing (DSP) systems using industry-standard DSP design methodologies.

"With each new generation of the System Generator tool, we've significantly enhanced design performance and productivity," said Omid Tahernia, vice president and general manager of the DSP Division at Xilinx. "The new tool, combined with the revolutionary DSP capability of the recently introduced Virtex-4 Platform FPGA family, takes the Xilinx XtremeDSP initiative to the next level and will drive FPGAs further into high performance DSP applications."

The System Generator v6.3i tool allows designers to take full advantage of the high performance features within the Virtex-4 Platform FPGA and the XtremeDSP Slice. Filters can be developed with speeds up to 500MHz at less than 1/10th the area than previous generation Xilinx FPGAs and at less than 1/7th the power in the signal processing chain.

The tool is also bridging the DSP tools gap by providing a complete, front-to-back design flow that blend the benefits of C-based and HDL design methodology within a single solution. System Generator v6.3i combines the benefits of C-based tools such as edit, compile, debug and quick design iterations with the benefits of HDL tools to create compact, high performance and highly parallel architectures. This allows designers with little or no experience in HDL design techniques to work at a very high level and go from first thought to verified silicon within a matter of days, rather than weeks.

A unique hardware in the loop co-simulation feature allows designers to greatly accelerate simulation while simultaneously verifying the design in hardware. System Generator v 6.3i includes a new DMA burst mode feature that increases data flow between the tool and FPGA by over 100 times - allowing designers to run multiple iterations in the time it took to run a single design in previous generation tools. The tool is also tightly coupled with the company's recently introduced Embedded Development Kit (EDK) v.6.3i, enabling designers to target Xilinx hard and soft processors and external processors for control path development.

"The Xilinx Virtex-4 FPGA and System Generator for DSP tool are an extremely powerful combination for designers of high-performance signal processing systems," said Ken Karnofsky, marketing director for Signal Processing and Communications at The MathWorks. "System Generator's high-bandwidth, DMA burst mode capability improves simulation time by over two orders of magnitude than previous generation tools."

System Generator for DSP Solution

System Generator automates the design, debug and deployment of FPGA-based processing systems with push-button performance. Systems architects, DSP engineers, and hardware designers can model complete

DSP systems in an integrated system-level design environment. In addition to the industry's richest simulation libraries for high level modeling and automatic validation code generation, System Generator provides a high-speed HDL co-simulation interface to the ModelSim simulator from Model Technologies, Inc. Other unique capabilities include MATLAB m-code compilation, fast system-level resource estimation, and high-speed hardware co-simulation interfaces, both a generic JTAG interface and PCI-based co-simulation for FPGA hardware platforms.

Comprehensive DSP Cores Library

In related news, Xilinx today announced the immediate availability of a DSP core library for use with its Virtex-4 Platform FPGA family. Through high levels of parameterization, the core library leverages unique Xilinx silicon capabilities like SRL16s and the XtremeDSP Slice to yield the fastest and smallest implementations in the FPGA industry. The new cores include a DOCSIS ITU-T J.83 Annex A/C Modulator core for cable modem head-end equipment and an enhanced Digital up-Converter (DUC) core for wireless infrastructure. The cores enable customers to develop faster, lower-cost designs for multi-carrier, spread spectrum and narrow-band systems.