Samsung's ViP Design Methodology Reduces SoC Design Time Up to 40 Percent

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Samsung Electronics Co., Ltd., a leader in advanced semiconductor technology, today revealed a hardware/software co-design methodology that will **reduce overall design time for the company's System-on-Chip (SoC) products by up to 40 percent**. The Virtual Platform (ViP) approach will ultimately result in faster production of Samsung logic components while giving the company's customers a time-to-market advantage.

Samsung developed the ViP design methodology in partnership with EDA vendors to address the ever increasing complexity of SoC design challenges. Today's exploding market for multi-function consumer products requires more on-chip firmware as well as transistors, complicating and extending the design process. Using the ViP methodology, simulation speeds are hundreds or even thousands of times faster than that of a traditional RTL approach while maintaining more than 90 percent of accuracy over RTL.

With the conventional RTL design methodology, it was not possible to design and optimize software before the field programmable gate array (FPGA) prototype is ready. In addition, it was hard to identify whether the error was due to hardware or software. Using the ViP approach, software designers can now prepare fully-optimized and error-minimized software before the development of RTL code, reducing the SoC design time by up to 40 percent.

Senior Vice President Soo-kwan Eo of the SoC R&D Center at Samsung

Electronics, who leads the ViP development team, said: “The ViP methodology has improved system design productivity and reduced SoC design and software development cycles. ViP will help us develop highly integrated devices ahead of the competition to maintain our market leadership.”

Some of Samsung’s SoC products have already benefited from the ViP methodology. It has been applied to develop the flash memory card controller that is already in mass production, enabling engineers to improve certain chip performance such as the data read operation by more than 30 percent.

Samsung’s ViP design methodology has proven its applicability to SoC products with multiple processors. For example, Samsung’s HD digital TV SoC, modem chip for 3G mobile phone, and mobile application processor devices have shown excellent results. Samsung will expand the use of ViP within its logic product line to encompass other various SoC devices.