Micron Qualifies 288 Megabit RLDRAM II Device

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Micron supports networking and video imaging markets with RLDRAM II products

Micron Technology, Inc., today announced qualification of the 288 megabit (Mb) reduced latency DRAM II (RLDRAM® II) products now available in volume production. RLDRAM II technology's fast random access, extremely high bandwidth and high density are optimal for high-performance networks, high-end commercial graphics, and server (L3) cache applications.

“We are very excited about RLDRAM II technology, and believe that RLDRAM II products will enable us to build higher performance and more cost effective products for our most demanding customers,” said Pradeep Sindhu, Vice Chairman and Chief Technical Officer of Juniper Networks. “Micron’s RLDRAM II technology is our architecture of choice for high-performance routing systems.”

“Micron’s RLDRAM II technology is approaching its one hundredth design win with applications requiring high bandwidth memories, DRAM-like densities, low latency, and fast internal cycle times,” said Achim Hill, Micron’s Senior Director of Marketing for Networking and Communication. “Realizing the overall system performance advantages derived from RLDRAM technology, many of our customers choose RLDRAM II technology as their high-performance memory. RLDRAM II product design activity continues to grow further validating it as the high-performance leader in the reduced latency technology market.”

Micron's RLDRAM II technology provides the best possible combination of bandwidth, low latency and reduced row cycle time (tRC) of 20 nanoseconds (ns), providing optimum bus utilization efficiency. Additional advantages of the RLDRAM II technology feature set include; on-die termination (ODT), multiplexed or non-multiplexed addressing, on-chip delay lock loop (DLL), common and separate I/O, programmable output impedance and a power efficient 1.8V core. These features offer designers optimum flexibility, providing a memory solution designed to fully optimize bus utilization whether the data bus is unidirectional or has a balanced READ and WRITE ratio.