Brand New 32-bit RISC Core

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Today, Cambridge Consultants launches a novel **32-bit RISC core that brings a new level of code density and power economy to deeply-embedded applications**. The XAP3 core is available in Verilog RTL and can be fabricated in under 50,000 gates in a variety of ASIC and FPGA technologies.

Unlike many other cores on the market, XAP3's instruction set has been optimized to exploit the code-efficient features of state-of-the-art C compiler technology, substantially reducing memory requirements and power consumption. In addition it supports position independent code and privileged modes, giving IC developers and their users a platform to create more versatile, robust, field-upgradeable products.

XAP3 is the latest addition to Cambridge Consultants' well-known XAP ASIC processor family. The XAP1 and XAP2 16-bit processors have been successfully used in consumer, wireless, industrial, healthcare and automotive products since 1995. For example, CSR the Bluetooth IC market leader uses XAP2 in all its BlueCore products. XAP3 continues Cambridge Consultants' policy of royalty-free licensing, making it the economic choice for use in high volume FPGAs, ASICs or ASSPs for all markets.

"We've amassed a great deal of experience in RISC processor technology from our previous XAP core designs and their use in commercial devices such as Bluetooth ICs and touchscreen controllers", says Alan Richardson, CTO of Cambridge Consultants. "By starting with a clean sheet of paper, we have been able to apply this know-how to

create a processor that really addresses the needs of the next wave of software-technology and connectivity-rich products using lean and power-efficient hardware with a simple and open programming structure".

XAP3 has a classic Von Neumann architecture allowing code and data to be freely mixed within its flat 4 Gbyte memory space. There is hardware support for position independent code and secure operation though privileged modes that prevent user programs from corrupting the operating system kernel. These features make XAP3 ideal for designing into high-volume, low-cost, high-reliability products that hold their programs in ROM or Flash.

XAP3 provides a level of performance that can easily handle the very complex software required for modern embedded systems while still retaining high code-density. This includes multi-tasking operating systems, real-time control, user interface, and communications stacks.

The new core's RISC instruction set, assembly language and ANSI C compiler have all been designed in parallel. The compile chain is based on Codemist C compiler technology, which has many novel features to optimize performance, while minimizing program size and memory requirements. Cambridge Consultants' designers then implemented the instruction set on the XAP3 core, and iterated the design to optimize its potential - providing single instructions for commonly-used functions such as function entry and exit. In conjunction with programmer-friendly hardware features such as XAP3's automatic selection of 16 or 32-bit wide instructions, the resulting platform achieves a remarkable code density, which Cambridge Consultants estimates could yield as much as a 30% saving in memory usage.

This not only reduces the hardware bill of materials, but power consumption as well - a critical feature for portable device applications.

Power economy is further reduced by XAP3's efficient power-down and interrupt modes. XAP3 also incorporates the sleep techniques already successfully used in XAP1 and XAP2.

XAP3 comes with an integrated programming and development environment called xIDE, comprising a compiler, linker, simulator and debugger. An xIDE integrated development environment for XAP3 will shortly join the xIDE toolkits for XAP1 and XAP2 that are already available for free 30-day trial download from www.CambridgeConsultants.com/ASIC.

XAP3 also includes Cambridge Consultants' patented SIF (serial interface) debug logic and interface that provides for non-invasive data acquisition, software development, real-time debugging and event monitoring.

A Linux real-time operating system port for XAP3 is underway. The XAP3 roadmap includes software support for the Nucleus OS, the GCC compiler (providing C++ and Java), and TCP/IP. This comprehensive set of hardware and software support will make it easy for developers to deliver complex semiconductor products on time with low risk.

"Because XAP3 programs are position independent, it is easy to locate them anywhere in memory with minimal load-time fix-ups. This will enable XAP3 systems to run multiple software applications or device drivers from different suppliers. It will be easy for software houses to publish new products for XAP3 hardware devices already in the field, thus creating a flourishing software market for this novel new platform" adds Alistair Morfey, head of Cambridge Consultants' ASICs group. "Privileged operating modes ensure that if any applets misbehave, they cannot corrupt the kernel. These features provide a versatile software platform that can be opened up to third parties, which will be a powerful differentiator for many emerging products."

XAP3 technology is licensed and delivered as a soft core in Verilog RTL code ready for designers to integrate into their product. Thereafter, Cambridge Consultants does not require royalty payments for devices sold with XAP3 inside. Cambridge Consultants also offers a wide range of complementary silicon IP and toolkits including configurable DSP cores, and analog and wireless IP components.

Details of the core are available at:
www.CambridgeConsultants.com/ASIC