

TI INTRODUCES INDUSTRY'S FIRST 3.3 V SUPPLY PECL/TTL TRANSLATORS

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Low-Voltage Devices Among Seven New PECL Products Replacing Discontinued Agere Devices

[Texas Instruments Incorporated \(TI\)](#) today introduced seven pseudo emitter-coupled logic (PECL) and translator/transistor logic (TTL) drivers and receivers, including the industry's first 3.3-V PECL translators and five devices that are direct replacements for translators discontinued by Agere Systems Inc. (Agere). The devices translate between differential input logic levels and TTL output logic levels. Designed for handling digital data or clock signals over balanced transmission lines, they are well-suited for applications such as telecommunications and medical imaging.

The 3.3-V TB3R1 and TB3R2 quad differential PECL receivers offer a low-voltage migration path for designers who have previously used 5-V supply PECL devices. Five other devices - the TB5D1M, TB5D2H, TB5R1, TB5R2 and TB5T1 - have combined features to replace nine former Agere PECL devices. The devices match the original Agere pinouts, allowing for plug-in replacement. Each new device offers 3-kV HBM and 2-kV CDM electrostatic discharge (ESD) protection and an operating temperature range of -40°C to 85°C.

Key Features:

Quad Differential PECL Drivers (TB5D1M and TB5D2H)

- Translate PECL input levels to TTL output logic levels
- 5.0-V or 3.3-V supply operation
- (TB5D1M) Surge protection on differential outputs
- (TB5D2H) No line loading when $V_{cc} = 0$
- Three-state output with a third-state level of less than 0.1 V
- Logic inputs include internal pull-up resistors of approximately 40 kOhm that are connected to V_{cc} to ensure a logical high level input if the inputs are open circuited.

Quad Differential PECL Receivers (TB5R1, TB5R2, TB3R1, TB3R2)

- Translate PECL input levels to TTL output logic levels
- 5-V supply (TB5R1, TB5R2)
- 3.3-V supply (TB3R1, TB3R2)
- 50 mV hysteresis (TB5R1, TB3R1)
- Preferred state output (TB5R2, TB3R2)
- Power-down loading characteristics of the receiver input circuit are approximately 8 kOhm relative to the power supplies to prevent loading the transmission line when the device is powered down.
- Enable inputs include internal pull-up resistors of approximately 40 kOhm connected to V_{cc} to ensure a logical high level input if the inputs are open circuited.

Dual Differential PECL Driver/Receiver (TB5T1)

- 5-V supply
- Translates TTL input levels to differential PECL output levels (driver) or converts PECL input levels to TTL output levels (receiver).
- Logic inputs include internal pull-up resistors of approximately 40 kOhm that are connected to V_{cc} to ensure a logical high level input if the inputs are open circuited.
- Power-down loading characteristics of the receiver input circuit are approximately 8 kOhm relative to the power supplies to prevent loading

the transmission line when the device is powered down.

- Each pair has its own common-mode enable control, allowing serial data and a control clock to be transmitted and received on a single circuit.
- In circuits with termination resistors, the line remains impedance-matched when the circuit is powered down.

The PECL translators join other TI interface and clocking products meeting designers' needs in PECL to TTL translation applications, such as the CDCM1804 and CDCM1802 clock buffers, each of which provides both a LVPECL output and a LVCMOS output.

For more information on finding the most appropriate bus interface solution for today's advanced system architectures, please refer to the "Comparing Bus Solutions" application report available at www.ti.com/sc04173b.

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