

Show Must Go On: Intel Keeps Moore's Law on Track with 65 nm Technology

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A significant **milestone in developing next-generation chip manufacturing technology** has been achieved by [Intel](#) Corporation. The company has built fully functional 70-megabit static random access memory ([SRAM](#)) [chips](#) with more than half a billion transistors using the world's most advanced **65 nanometer (nm)** process technology. The achievement extends Intel's effort to drive the development of new manufacturing process technology every two years, in accordance with Moore's Law.

The transistors in the new 65nm (a nanometer is one-billionth of a meter) technology have gates (the switch that turns a transistor on and

off) measuring 35nm, approximately 30 percent smaller than the gate lengths on the previous 90nm technology. For comparison, about 100 of these gates could fit inside the diameter of a human red blood cell.

The new process technology increases the number of tiny transistors squeezed onto a single chip, giving Intel the foundation on which to deliver future multi-core processors, and to design innovative features into future products, including virtualization and security capabilities. Intel's new 65nm process technology also includes several unique power-saving and performance-enhancing features.

"Intel continues to meet the increasing challenges of scaling by innovating with new materials, processes and device structures," said Sunlin Chou, senior vice president and general manager of Intel's Technology and Manufacturing Group. "Intel's 65nm process technology has industry-leading density, performance and power reduction features that will enable future chips with increased capabilities and performance. Intel's 65nm technology is on track for delivery in 2005 to extend the benefits of Moore's Law."

In November 2003, Intel announced it used its 65nm process to build 4-megabit SRAMs. Since that time, the company has fabricated fully functional 70-megabit SRAMs on this process with a very small die area of 110 mm². Small SRAM cells allow for the integration of larger caches in processors, which increases performance. Each SRAM memory cell has six transistors packed into an area of 0.57 μm^2 . Some 10 million of these transistors could fit in one square millimeter, roughly the size of the tip of a ball point pen.

New Power-Reduction Features for 65nm Technology

According to Moore's Law, the number of transistors on a chip roughly doubles every two years, resulting in more features, increased

performance and decreased cost per transistor. As transistors get smaller, increased power and heat dissipation issues develop. As a result, implementing new features, techniques and structures is imperative to continuing this progress. Intel has addressed these challenges by integrating power-saving features into its 65nm process technology. These features are critical to delivering power-efficient computing and communication products in the future.

Intel's leading **strained silicon technology**, first implemented in its 90nm process technology, is further enhanced in the 65nm technology. The second generation of Intel strained silicon increases transistor performance by 10 to 15 percent without increasing leakage. Conversely, these transistors can cut leakage by four times at constant performance compared to 90nm transistors. As a result, the transistors on Intel's 65nm process have improved performance without significant increase in leakage (greater electrical current leakage results in greater heat generation).

Intel's 65nm transistors have a reduced gate length of 35nm and a gate oxide thickness of 1.2nm, which combine to provide improved performance and reduced gate capacitance. The reduced gate capacitance ultimately lowers a chip's active power. The new process also integrates eight copper interconnect layers and uses a "low-k" dielectric material that increases the signal speed inside the chip and reduces chip power consumption.

Intel has also implemented "sleep transistors" in its 65nm SRAM. Sleep transistors shut off the current flow to large blocks of the SRAM when they are not being utilized, which eliminates a significant source of power consumption on a chip. This feature is especially beneficial for battery-powered devices, like laptops.

"Intel has been actively working on the power and heat dissipation

challenges faced by the semiconductor industry," Chou said. "We have taken a holistic approach by developing solutions that involve systems, chips and technologies, and include innovations on our 65nm technology that go beyond simply extending prior techniques."

Intel's 65nm semiconductor devices were manufactured at the company's 300mm development fab (called D1D) in Hillsboro, Ore., where the process was developed.

More information on Intel's 65nm logic technology will be presented in a paper at the IEEE International Electron Devices Meeting in San Francisco Dec. 12-15. Additional information can also be found on Intel's Silicon Showcase at <http://www.intel.com/research/silicon>.

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