Infineon Demonstrates Next Generation Server Memory Modules: First Test Chip for Fully Buffered DIMMs

August 10 2004

Infineon Technologies AG (FSE/NYSE: IFX) today announced that it has successfully tested the industry's first advanced memory buffer (AMB) test chip for next generation server modules using Double Data Rate2 (DDR2) Dynamic Random Access Memory (DRAM). The AMB is the central part of fully buffered dual in-line memory modules (FB-DIMMs), which will be the new standard for server memory. By combining its in-house expertise in high-frequency chip design and DRAM technology to implement a complete solution Infineon gains a leadership position in the development of AMBs and FB-DIMMs.

The continuous introduction of high speed DRAM technologies from DDR2 to DDR3, and the increasing amount of data stored and processed in servers poses technical challenges that require a novel and innovative server memory architecture. Memory modules used today have parallel direct access to the bus (multi-drop-bus architecture). The FB-DIMM channel architecture introduces point-to-point connections between the memory controller and the first module on the channel, and between subsequent modules down the channel. This makes the bus-loading independent from the DRAM input/output (IO) speed and thereby enables high memory capacity with high-speed DRAMs. The AMB chip located on each FB-DIMM collects and distributes the data from or to the DRAMs on the DIMM, buffers the data internally on the chip and forwards or receives it to the next DIMM or memory controller. Hence, the buffer chip is the crucial point in the development of the new FB-

DIMM memory architecture.

”We are committed to become the industry leading vendor for fully buffered DIMM and expect to realize a major sales share with this high margin and high volume product targeting the server and workstation markets,“ said Dr. Carsten Gatzke, Senior Director Product Marketing of Infineon’s Memory Products business group. “Infineon’s combined know-how in high-frequency chip design and its extensive DRAM expertise are the driving forces behind the currently achieved significant milestone,” added Christian Scherp, Vice President and General Manger of Infineon’s North America Wireline Communications Business Group. “We will use this extensive competence to boost further development of advanced memory buffers and address emerging markets with our leading edge solution.”

”The new fully-buffered technology, with a specification standardized in Jedec (Joint Electronic Device Engineering Council), provides an excellent opportunity to simultaneously increase both the speed of the DIMMs and the memory capacity on server platforms. FB-DIMM will also offer a smooth transition from DDR2 to DDR3 DRAM generations. This has the real potential to be an important new server memory technology in 2006 and onwards,” said Tom Macdonald, Vice President and General Manager of the Advanced Chipset Division at Intel. ”Suppliers of server equipment recognize the need for a long-term buffered DRAM memory solution and the industry enabling activities with companies like Infineon Technologies will accelerate and ease the introduction of such an innovative and high-performing memory technology.”

The Infineon AMB test chip implements for the first time the crucial high-speed input/output stages together with other high-speed functionality such as the data-insertion and data-forwarding circuits in Infineon’s own logic process technology. The FB-DIMM standard

foresees a data multiplexing by a factor of six to higher speeds to reduce the physical width of the memory channel and to minimize the throughput latency. The Jedec standard defines a maximum required datarate per IO pin of 4.8 Gb/s for DDR2 800. Infineon's AMB test chip already runs at 6.0 Gb/s, giving substantial system margin and ensuring lowest bit-error rates. By achieving this major development milestone Infineon can now further optimize the circuit design with real-world measured data.

Engineering samples of the FB-DIMM for DDR2 DRAM are planned to be available in the fourth quarter of 2004, market introduction is planned for the second half of 2005.

Source: Infineon