Fujitsu Ties Global Partnership with Cadence to Create Advanced SoC Design Environments

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Faster design turnaround time for large-scale chips at 0.13 micron and beyond

Fujitsu Limited and Cadence Design Systems, Japan today announced a global partnership agreement under which they will create advanced system-on-chip (SoC) design environments. The design environments resulting from this agreement will further address today's demand for new design methodologies for the development of advanced SoCs.

Currently there is an urgent need for new design methodologies for the development of advanced SoCs, particularly for the latest SoC designs that incorporate process technologies of 90nm (nanometer) and beyond. The semiconductor industry's rapid product cycles are driven by constant technological advances and are subject to volatile market fluctuations. This makes it increasingly difficult to keep pace with the latest design environment requirements and quickly deploy new design methodologies to worldwide design facilities.

The Premier Design Partner agreement(1) that Fujitsu and Cadence have entered into is anticipated to strengthen Fujitsu's design approach with shorter design lead times and improved design quality. This partnership agreement is revolutionary as an EDA (Electronic Design Automation)(2)-related agreement, as it provides design solutions that go beyond a simple sales agreement for EDA tools.

Highlights of the agreement are as below:

- The agreement encompasses tens of thousands of Cadence licenses, including numerous SoC Encounter™ licenses.
- The worldwide Fujitsu Group and all of its design centers will have access to licenses covered by this agreement.
- In addition to its standard support, Cadence will provide personnel support organizationally to the worldwide Fujitsu Group and its design centers in order to fully leverage this agreement.

As strategic business partners, Fujitsu and Cadence will jointly develop methodologies that merge design and process technologies, and plan to expand their global business collaboration to markets such as in the U.S. and China.

Under this agreement, Fujitsu will deploy to all of its design centers the combination of a variety of licenses and a new design methodology known as physical prototyping (also referred to as silicon virtual prototyping)(3) for SoC development for 0.13micron technology and beyond. Using the world's highest-standard design environments will minimize design iterations, which can be a major obstacle for meeting delivery deadlines, and will significantly shorten design lead times. This approach is also highly effective for reducing die size and noise, and lowering power consumption.

These advantages make it possible for Fujitsu to finalize and fix SoC design schedules, which are of particular importance to customers, and also contribute greatly to the finalization of customers' tight product development schedules.

As a SoC design technology partner that goes beyond being a conventional EDA supplier, Cadence will support Fujitsu's SoC business by establishing an internal organization dedicated to provide centralized support to Fujitsu's design centers worldwide.

Shigeru Fujii, Senior Corporate Vice President and Group President of Fujitsu Limited's LSI Business Group said, "For the latest technology, while LSI functions continue to grow in complexity and become larger in scale, and design and development become increasingly difficult, there is a great need for shortening development lead times. In order to overcome these issues, Fujitsu is implementing a new IDM (Integrated Device Manufacturer) business model in which we establish strategic partnerships with customers and vendors. This agreement with Cadence is a facet of this new IDM business model. We will help our customers increase their product competitiveness by updating our development environments to the world's highest standards."

General Manager of Fujitsu Limited's Design Methodology Development Division, LSI Group, Kazuyuki Kawauchi states, "Under this agreement with Cadence, all of our design centers and the Fujitsu Group worldwide will be equipped with abundant EDA tools as well as new design methodologies to fully leverage them. It is now possible to overcome and resolve the issue of design iterations, the most challenging issue for developing large-scale SoCs using 0.13 micron technology and beyond, thus enabling us to dramatically raise the certainty of design schedules. Now that this agreement is in place, I strongly believe that the days when our design environments were limited by the number of tools available will be a thing of the past."

"Cadence will support Fujitsu's SoC business with a complete solution ranging from upper-stream to lower-stream designs, implementation, verification and manufacturing", said Ryoichi Kawashima, President of Cadence Design Systems, Japan. "This innovative agreement is unique in its large-scale, comprehensive, enterprise-level approach - the likes of which no other EDA company has ever offered. We are committed to support Fujitsu in all of its many design centers worldwide."

Glossary and Notes

(1) Premier Design Partner agreement: Cadence's Premier Design Partner Agreement expands the customer relationship beyond tools to include complete business solutions to customers. It includes establishing business models that directly contribute to customers' business success by helping reduce their total cost of ownership, minimizing design risks and optimizing the design chain.
(2) EDA (Electronic Design Automation): Technology that automates the design of various electronic systems, and the semiconductors and printed circuit boards that such systems are comprised of.
(3) physical prototyping (also referred to as silicon virtual prototyping): A SoC design methodology that detects problems and implements measures to address those issues, prior to circuitry layout. This approach enables minimizing the need for design iterations, which with conventional design methods could take more than several months. This methodology also makes it possible to reduce design processes, improve level of certainty of estimated design lead times, and enables early determination of best conditions in regard to power consumption and chip size. Cadence's SoC Encounter ™ facilitates physical prototyping.

The original press release can be found here.