Airgo Networks Manages Power for Complex Wireless SoC Design with Sequence's PowerTheater

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RTL and Gate Analysis Used to Accelerate Market Introduction of Innovative Wi-Fi Application

Airgo Networks, a developer of innovative wireless technology and products, "taped-out" using Sequence Design's PowerTheater to automate power analysis for its revolutionary 802.11g chips. "PowerTheater predicted power usage within 10% of silicon for our AGN100BB chip. We achieved this level of accuracy by leveraging PowerTheater's innovative RTL and gate-level analysis capabilities," said Derrick Lin, senior director of ASIC engineering at Airgo Networks.

Since switching to PowerTheater's accurate and automated RTL power estimation, Airgo designers have minimized power early in the design cycle and verified that power budgets are met.

"We are pleased that Airgo, a leader in the hot Wi-Fi space, has adopted PowerTheater for its high performance chipsets," said Vic Kulkarni, Sequence president and CEO. "Power has become design enemy #1, illustrating the need to manage power consumption effectively through a comprehensive RTL to gate approach."

PowerTheater is the initial step in Sequence's NanoCool low-power design flow. The flow includes RTL power analysis, voltage-drop analysis and optimization, as well as, leakage power reduction. Details

may be found at:
www.sequencedesign.com/2_solut … NC-DataSheet_New.pdf

Sequence recently launched the NanoCool Low-Power Design seminar series with co-sponsors Artisan Components and Sun Microsystems. Attendees packed the historic Silicon Valley Capital Club Athletics to learn about power management at ESL, RTL and gate-level, with a particular emphasis on leakage power reduction. Inquiries for seminar proceedings should be addressed to seminars@sequencedesign.com.

About PowerTheater

With the rapid growth of mobile applications markets, power dissipation is an increasing concern in system-on-chip (SoC) designs. With 80% of current design starts constrained under 2W of power, power management is in the forefront of design challenges. Typically 80% of the power in these designs is determined at the RTL stage or earlier. Power actions taken early, before synthesis, save significantly more power overall. Sequence is the first company to offer fast, accurate RT and gate level design solutions that analyze and reduce power dissipation in complex SoC designs. PowerTheater is a family of full-chip power tools that can be used throughout the IC design process. PowerTheater products analyze, display and help the user reduce power for the whole chip and each individual module. Accuracy is achieved through a combination of special-purpose estimation algorithms and carefully crafted modeling techniques.

PowerTheater provides the foundation for a comprehensive SoC power management methodology. Highlights include:

- SoC RTL Power Analysis
- Low power RTL design
- Flexible and Easy-to-Use RTL Power Optimization

- Handle Clock, Memory, Data Path Control Logic and I/O
- De Facto Industry Standard for RTL Power Design
- Complete HDL coverage for SoC design
- Versatile Graphical Analysis Environment
- Accurate Gate-Level Power Verification

PowerTheater has considerable momentum in the marketplace with endorsements from users such as Ricoh, Samsung, Tensilica, Sun and Amphion. The product is part of the LSI Logic FlexStream Design Solution, and is integrated into IBM's Blue LogicTM ASIC design system.

Source: Sequence