Renesas Technology Releases SH7780 Microprocessor Incorporating SH-4A SuperH CPU Core and PCI Bus Controller

July 22 2004

Renesas Technology Corp. today announced the development of the SH7780, a 32-bit microprocessor incorporating the SH-4A, the high-end CPU core in the SuperH™* 1 Family, and a PCI bus * 2 controller (PCIC). It is designed for high-performance multimedia applications such as game machines, digital home electronics products, and car navigation systems. Sample shipments will begin in November 2004 in Japan .

The SH7780 is the successor to the existing SH7751R, which incorporates a SH-4 core and a PCI bus controller.

Features of the SH7780 are summarized below.

(1) Incorporating high-performance SH-4A, the high-end CPU Core in the SuperH Family and the performance of 720 MIPS
The SH-4A CPU core has a maximum operating frequency of 400 MHz and realizes processing performance of 720 MIPS. It is approximately 1.7 times as fast as existing SH-4 CPU core operating at 240 MHz. The four-way set-associative cache memory is divided into two 32-Kbyte areas, one for instructions and one for data. This results in an improved cache hit ratio in comparison with existing products based in the SH-4 core. The faster software processing speed contributes to an overall increase in system performance. The instruction set is fully SH-4 upward compatible. This makes it possible to utilize existing program and helps

reduce system development time.
In addition, the SH7780 incorporates an on-chip floating point unit (FPU) with a maximum operating speed 400 MHz. The FPU supports both single-precision and double-precision arithmetic operations and delivers a maximum processing performance of 2.8 GFLOPS when operating in single-precision mode. Furthermore, hardware support for sine/cosine arithmetic operations contributes to high-speed rendering of 3-D graphics.

(2) On-chip PCI bus controller for excellent system expandability
The SH7780 incorporates an on-chip 32-bit PCI bus controller . This makes it possible to connect the microprocessor to a PCI bus, the type of general-purpose bus commonly used in PCs. In addition, the PCIC supports the PCI Rev. 2.2, allowing connections with LSI devices incorporating PCI interface and operating at either 66 MHz or 33 MHz. This makes it possible to use low-cost external devices such as PC peripherals.

(3) Three kinds bus (DDR-SDRAM memory bus, PCI bus, local bus) architecture for superior system performance
The SH7780 employs three kinds of bus: a 32-bit bus for connections to double data rate synchronous DRAM (DDR-SDRAM), a 32-bit bus for PCI bus connections, and a 32-bit local bus for connecting to flash memory, SRAM, etc. These three external buses can be operated simultaneously, allowing for efficient data transfer and improved performance. The result is enhanced system performance overall.

In recent years game machines fields have come to offer diverse and expanded display capabilities combining 2-D and 3-D graphics. In addition, there are tends toward advanced user interfaces with sophisticated speech recognition and speech synthesis capabilities, high-level image recognition functionality, and the like. Furthermore,

automobile information terminals, such as car navigation systems, now incorporate functionality for connecting to the Internet using a mobile phone and downloading and displaying constantly-updated information on the weather, local restaurants, news, and the like. As automobile information terminals become more diverse and their performance demands increase, the system software they employ is becoming ever more complex.

Such products are expected to implement still higher levels of performance and add more new functions in the years ahead. As such, the ability to utilize existing software resources when developing new systems is very important.

Renesas Technology responds to this need with the SH7780, with is built around the newly developed SH-4A CPU core. It offers instruction upward-compatibility with the SH-4 CPU core employed in previous generations of widely used microprocessors. In addition to the SH-4A CPU core, the high-performance SH7780 microprocessor implements a PCI bus controller and many other on-chip peripheral functions.

The SH-4A is a newly developed CPU core. Its maximum operating frequency is 400 MHz - 1.7 times that of the existing SH-4 core, which operates at a maximum of 240 MHz - and achieves a maximum processing performance of 720 MIPS. In addition, it has a 32 Kbytes four-way set-associative instruction cache and a 32 Kbytes four-way set-associative data cache. This enables it to deliver a higher cache hit ratio than products based on the SH-4 CPU core and results in faster software processing. The SH-4A thus provides support for a new generation of high-performance multimedia systems. In addition, the instruction set is upward compatible with the SH-4. This means that existing program can be utilized and contributes to sorter system development time. Furthermore, the SH-4A CPU core incorporates an FPU that supports both single-precision and double-precision arithmetic operations. The

FPU is 1.7 times as fast as the FPU in the existing SH-4, which operates at 240 MHz, and it achieves maximum processing performance of 2.8 GFLOPS when operating in single-precision mode. Also, hardware support for sine/cosine arithmetic operations contributes to high-speed rendering of 3-D graphics.

The SH7780 incorporates an on-chip 32-bit PCI bus controller for making connections to a PCI bus, the type of general-purpose bus commonly used in PCs. The PCI bus controller supports the PCI Rev. 2.2, allowing connections with LSI devices incorporating PCI interfaces and operating at either 66 MHz or 33 MHz. This makes it possible to use low-cost external devices such as PC peripherals, thereby contributing to reduced overall system cost.

To increase data transfer performance, the SH7780 has three kinds of bus. A 32-bit bus allows connection with DDR-SDRAM, which is faster than single data rate synchronous DRAM (SDR-SDRAM); a 32-bit bus supports PCI bus connections; and a 32-bit local bus allows for connections to flash memory, SRAM, etc. The three external buses can be operated simultaneously. This permits more efficient data transfer than existing products that employed a single bus for connections to main memory and as the local bus, and which did not support simultaneous operation.

In addition to the cache memory, the SH7780 has 16 Kbytes of on-chip high-speed RAM that can be allocated for either programs or data that require high-speed access. Real-time system performance can be improved by using this RAM to store exception handling routines, or the like.

Also implemented on-chip peripheral functions in the SH7780 are an interrupt controller (INTC), a real-time clock (RTC), a watchdog timer (WDT), and an interface for connecting to an audio CODEC IC, in

addition to other peripheral modules such as a serial interface.

The package is a 449-pin BGA (21 mm × 21 mm) and the device's external dimensions are approximately 60% reduced than SH7751R. This is useful for designers of compact systems.

The E10A-USB emulator, which connects to a host PC via a universal serial bus (USB) connection, is available as a development environment. In addition, the SH7780 has an on-chip debugging function that allows debugging at the maximum operating frequency.

In the years ahead Renesas Technology will continue to respond in a timely manner to market requirements by developing high-speed CPU products offering increased performance and an expanded range of functions.

Notes: 1. SuperH is a trademark of Renesas Technology Corp.
2. PCI (Peripheral Component Interconnect) is a bus standard established by the PCI Special Interest Group.

* Other product names, company names, or brands mentioned are the property of their respective owners.

Game machines, digital home electronics products, industrial equipment, etc.
Automobile information terminals: Car navigation systems, etc.

The original press release can be found here.