MoSys' 1T-SRAM-Q Memory Silicon-Verified on Chartered's 0.13-Micron Industry Standard Logic Process

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MoSys, Inc. (Nasdaq:MOSY), the industry's leading provider of advanced high density embedded memory solutions, and Chartered Semiconductor Manufacturing (Nasdaq:CHRT) (SGX:CHARTERED), one of the world's top three dedicated semiconductor foundries, today announced the silicon validation of MoSys 1T-SRAM-Q(TM) (Quad density) embedded memory technology on Chartered's 0.13-micron industry-standard logic process. Their joint efforts have produced functional silicon devices and already resulted in new design engagements with mutual customers. The final phases of qualification are underway with full characterization data to be available by the end of the third quarter 2004.

With a complete macro density of approximately 1.2-square millimeters per megabit, 1T-SRAM-Q technology enables designers to embed even larger high-performance memories in their system-on-chip (SoC) designs. 1T-SRAM-Q technology incorporates MoSys' proprietary Transparent Error Correction(TM) (TEC(TM)) technology delivering the additional benefits of improved yield and reliability with elimination of laser repair and soft error concerns.

"Chartered's 0.13 silicon verification of 1T-SRAM-Q memory demonstrates MoSys' continued commitment to develop the best-in-class memory technology," commented Dr. Fu-Chieh Hsu, president and CEO of MoSys. "Now, SoC designers can integrate over 100 megabits of high-

performance embedded memory in 0.13-micron designs."

1T-SRAM-Q memory is based on MoSys' patented Folded Area Capacitor(TM) (FAC (TM)) technology to reduce bit cell size by literally folding the bit cell gate oxide capacitor vertically down the STI sidewall, thus dramatically reducing the horizontal area. This results in typical bit cell sizes of 0.57 square microns at the 0.13-micron process node.

"The memory requirements of our customers are increasing over time and with each technology node. By coupling MoSys' high-density embedded memory technologies with our production-proven 0.13-micron process, we're giving designers more choices," said Kevin Meyer, vice president of worldwide marketing and services at Chartered. "With access to these world-class solutions, our customers can reduce the risks of implementing leading-edge, memory-intensive SoCs and still target the highest possible yields."

The 1T-SRAM-Q validation effort is an extension of the ongoing collaboration by the two companies to offer optimized high-density memory solutions on multiple technology generations and products. MoSys and Chartered have already successfully qualified MoSys' 1T-SRAM-R high-density memory solution on Chartered's 0.18-micron and 0.13-micron process technologies. The companies are in the process of qualifying the 1T-SRAM-R technology on the 90nm process platform jointly developed by Chartered and IBM.

Source: www.charteredsemi.com/

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