Cypress Announces Silicon Valley Technology Center with 65-nm Fab

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SAN JOSE, Calif., July 6, 2004 – Cypress Semiconductor Corp. today formally opened **the Silicon Valley Technology Center** (SVTC), a facility that offers start-up and established corporations the opportunity to develop and characterize their silicon-based technologies cost-effectively, accelerating time to revenue. SVTC customers will have access to Cypress's **65-nanometer state-of-the-art Research and Development fab in Silicon Valley**. They will be able to take advantage of Cypress's 20+ years of technology development and design experience.

"SVTC offers its customers an alternative strategy for taking a product from proof-of-concept to manufacturing," said Chris Seams, executive vice president of technology and worldwide manufacturing for Cypress. "SVTC offers access to state-of-the-art equipment, a broad process-module library, and 22 years of established R&D infrastructure—a combination you will not find in a university lab. This is a valuable asset for customers trying to characterize their new technology for manufacturing, where adding new value to the silicon base will be key to differentiation and success."

Customers will use SVTC's process and materials expertise to develop novel silicon technology for integrated circuits, microelectromechanical systems, and applications incorporating new nanotechnology and biotechnology processes. SVTC aims to expand its business model to duplicate successes with current customers, such as Matrix Semiconductor, which produces Matrix® 3-D Memory (3DM) ¾ the

first three-dimensional, high-density, low-cost, nonvolatile memory for portable electronic devices. Matrix used SVTC to develop the first high-volume approach to making Matrix 3DM before transferring its technology successfully to a foundry-manufacturing environment.

“SVTC has enabled Matrix to build prototypes that have transferred successfully to our foundry quickly and cost-effectively—something we were unable to do in a pure lab environment,” said Siva Sivaram, chief operating officer of Matrix Semiconductor. “SVTC experts handled all the wafer manufacturing and equipment maintenance, which allowed us to focus on our product design.”

SVTC customers share an established fab infrastructure with other companies in a secure intellectual property environment. SVTC provides fab activities on state-of-the-art equipment in a high-quality environment executed by highly-skilled R&D technicians and operators. Additionally, SVTC offers best practices in fab process engineering, statistical process control, failure analysis, and design for manufacturing methodologies as part of its development toolbox.

The original press release can be found here