# TOSHIBA TO START PRODUCTION OF INDUSTRY'S FIRST SOC WITH THE X ARCHITECTURE

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Implementation of the X Architecture enables higher performing, smaller devices for digital-media and home-entertainment applications

SAN DIEGO, CALIF. and TOKYO, June 7, 2004 -- Marking a significant milestone, the X Initiative, Cadence Design Systems, Inc. (NYSE:CDN) and Toshiba Corporation announced today that Toshiba has launched the industry's first commercial system-on-chip (SoC) devices built on the innovative X Architecture design-a new approach to large-scale integration that enables the production of smaller, faster chips. Toshiba's latest TC90400XBG chip validates the benefits of the X Architecture by delivering a powerful, compact and highly integrated solution for next generation digital video broadcast and multimedia home-entertainment applications.

The X Architecture represents a new way of orienting a chip's microscopic interconnect wires with the pervasive use of diagonal routes, in addition to traditional right-angle "Manhattan" routing. This innovative architecture results in chip designs with significantly fewer wires and less vias to connect the wiring layers in SoC devices. By enabling higher quality device performance metrics, the X Architecture will bring significant advantages to next-generation digital media and other advanced consumer applications. Toshiba and Cadence have collaborated on the development of the X Architecture and are co-sponsors of the X Initiative, a consortium of more than 40 leading

companies dedicated to facilitating the commercial adoption of the X Architecture by preparing the design chain for volume production.

Toshiba's milestone chip, TC90400XBG, designed for integration in digital-media and home-entertainment applications, is fabricated with 130-nanometer process technology. Compared to equivalent Toshiba products with the conventional "Manhattan" design, the new chip implementing the X Architecture is approximately 11 percent faster in speed and 10 percent smaller in random logic area. Samples of the new chip will be available in November 2004 and mass production is expected to begin in the second quarter of 2005. Toshiba has already won its first customer for TC90400XBG: the chip will be integrated into digital TVs, initially in products for the European market.

Commenting on the importance of the milestone for both Toshiba and the X Initiative, Takashi Yoshimori, Technology Executive SoC-Design of Toshiba's Semiconductor Company, said, "By collaborating with Cadence and members of the X Initiative to develop the industry's first X-based SoC, Toshiba is responding to diversifying market demands for performance-enabling single-chip solutions that can result in faster and smaller chips when compared to conventional design methodologies. With the application of this state-of-the art design process, Toshiba will further leverage its leadership in the SoC market."

"Toshiba has played an integral role in advancing the commercial viability of the X Architecture, including the development of the first 90-nm functional test chip (announced last year at the CEATEC Exhibition in Japan)," said Aki Fujimura, X Initiative steering group member and CTO, new business incubation at Cadence. "We are delighted that this design architecture is clearly proving to be a very advantageous choice for leading design applications such as digital media technology. We see this as the next step toward production of the X Architecture as it paves the way toward broad commercial adoption by

the global semiconductor industry."

About the X Architecture

The X Architecture, the first production-worthy approach to the pervasive use of diagonal interconnect, reduces the total interconnect, or wiring, on a chip by more than 20 percent and via-counts by more than 30 percent, resulting in simultaneous improvements in chip performance, power and cost. For the past 20 years, chip design has been primarily based on the de facto industry standard "Manhattan" architecture, named for its right-angle interconnects resembling a city-street grid. The X Architecture rotates the primary direction of the interconnect in the fourth and fifth metal layers by 45 degrees from a Manhattan architecture. The new architecture maintains compatibility with existing cell libraries, memory cells, compilers and IP cores by preserving the Manhattan geometry of metal layers one through three.

About the X Initiative

The X Initiative, a group of leading companies from throughout the semiconductor industry, is chartered with accelerating the availability and fabrication of the X Architecture, a revolutionary interconnect architecture based on the pervasive use of diagonal routing. The X Initiative's five-year mission is to provide an independent source of education about the X Architecture, to facilitate support and fabrication of the X Architecture through the semiconductor industry design chain, and to survey usage of the X Architecture to track its adoption. Representing leaders spanning the entire design-to-silicon supply chain, X Initiative members include: Applied Materials, Inc.; ARM; Artisan Components, Inc.; ASML Netherlands B.V.; Cadence Design Systems, Inc.; Canon U.S.A. Inc.; Dai Nippon Printing (DNP); DuPont Photomasks, Inc.; Etec Systems, Inc., an Applied Materials, Inc. company; GDA Technologies, Inc.; HPL Technologies, Inc.; Hoya

Corporation; IN2FAB Technology Ltd.; Infineon Technologies AG; JEOL, Ltd.; KLA-Tencor Corporation; Leica Microsystems AG; Matsushita Electric Industrial Co., Ltd.; MicroArk Co. Ltd.; Monterey Design Systems, Inc.; Nikon Corporation; NuFlare Technology Inc.; PDF Solutions, Inc.; Photronics, Inc.; Prolific Inc.; RUBICAD Corporation; Sagantec; Sanyo Electric Co., Ltd.; Silicon Logic Engineering, Inc.; SiliconMap, LLC.; Silicon Valley Research Inc.; STMicroelectronics; Sycon Design, Inc.; Tensilica, Inc.; Toppan Printing Co.; Toshiba Corporation; Trecenti Technologies, Inc.; TSMC; UMC; Virage Logic, Inc.; Virtual Silicon Technology, Inc.; and Zygo Corporation. Membership is open to all companies throughout the semiconductor supply chain. Materials can be found at www.xinitiative.org

The original press release can be found here.