TI DDR Memory Power Design With Integrated Switcher and LDO Enhances Power Performance and Minimizes Cost

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Designers that use double data rate (DDR) and DDR II memory systems can now incorporate Texas Instruments´ (TI) new integrated circuit (IC) that combines a DC/DC switch-mode controller and linear dropout (LDO) regulator to enhance power performance. The highly integrated device significantly reduces the number of external components typically required to support all the power management for DDR systems, such as Micron´s DDR and DDR II systems, in applications such as notebook and desktop computers, graphics cards and game machines

"End-equipment manufacturers are steadily designing newer products that support denser memory systems, while not sacrificing battery life," said Terry Lee, Executive Director of Advanced Technology and Strategic Marketing for Micron's Computing and Consumer Group. "We are working with a handful of leading semiconductor companies, such as Texas Instruments, who are able to offer advanced power management analog technology that combines the right level of integration, versatility and high performance to quickly meet changing power requirements of next-generation DDR memory systems."

TI´s new TPS51116 integrates a synchronous current mode DC/DC controller to power Vddq, a 3-A LDO regulator to power Vtt and a buffered reference, Vref. Fully compliant to DDR and DDR II JEDEC specifications, a complete DDR power solution can be achieved by including the power train for the switcher, and adding as few as seven

external resistors and capacitors - compared to today´s systems that use 18 or more separate power management components. The TPS51116 has excellent light load efficiency, achieving greater than 85 percent Vddq efficiency at 10mA. The high performance LDO can sink/source 3-A peak currents while only needing a 2x10-µF ceramic output capacitor.

The switcher inside the TPS51116 employs a control technique called D-CAPTM mode to supply 100 nanoseconds (ns) of load-step transient response and reduce the number of external output capacitors. D-CAP mode also eliminates the need for external loop compensation; however, if more control is required, loop compensation for the TPS51116 can be changed to support any output capacitor type, including ceramic. The integrated LDO requires 2x10-µF ceramic output capacitors, and can significantly reduce power dissipated in the system by reducing its input voltage. Capable of supporting many design types, Vddq voltage level can be adjusted or fixed at 2.5 V for DDR and at 1.8 V for DDR II.

Sleep State Improves Time to Market and Memory Reliability

In addition to high performance, the TPS51116 manages sleep state control functionality to help improve reliability to the DDR memory system. This integrated feature improves time to market by designing the control functions internally as opposed to the added time of designing externally. In addition, the TPS51116 ensures Vtt is less than Vddq, which further improves DDR memory reliability.

Key Technical Features of the TPS51116:

Wide Input Voltage Range: 3 V to 28 V
D-CAP Mode with 100-ns Load Step Response
Accuracy +/- 20-mV for Vtt & Vref

Sleep Mode Operation with Selectable Soft-off for Output Discharge
Requires only a 2x10-µF Ceramic Output Capacitor for Vtt
Thermal Shutdown, Power Good, Over Voltage Protection, Under Voltage Protection
Compliant to both DDR and DDR II JEDEC Specifications

New 3-A Termination Regulator for Space-Constrained Systems

In addition to the highly integrated TPS51116, TI has released a 3-A sink/source tracking termination regulator in a 10-pin MSOP package, specifically designed for low-cost DDR and DDR II systems where space is a premium. The TPS51100 includes many of the same features as the LDO portion of the TPS51116 device, including 2x10-µF ceramic output capacitors and remote sensing functions. The input to the 3-A termination regulator can be reduced to help reduce the total power dissipation in the system