TEXAS INSTRUMENTS RESEARCHERS OUTLINE PATHS TO REDUCE CHIP POWER CONSUMPTION, INCREASE PERFORMANCE

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Technical Disclosures Present New Options for Chip Scaling

DALLAS (June 15, 2004) - Texas Instruments Incorporated announced its semiconductor research teams have developed cost effective techniques to dramatically lower chip power consumption and a new approach to increase overall performance. TI's new power management technologies can reduce leakage power from idle transistors by a factor of 1000, while unique strained silicon techniques can increase transistor performance by 35 percent. The developments are being presented in two technical papers at the respected Symposium on VLSI Technology this week in Honolulu, Hawaii.

"TI builds chips covering things from battery powered consumer products to high-end server microprocessors. Supporting that large range of applications requires different production processes that deliver the right balance of power and performance," said Dr. Hans Stork, TI's Chief Technology Officer. "Our researchers are presenting at the VLSI Symposium unique approaches we plan to bring to production that push both the low power and high performance envelopes without negatively impacting cost."

Controlling Power

Low-power semiconductor design has becoming increasingly critical as more multimedia and high-end digital consumer electronic features are integrated onto System-on-Chip (SoC) products found in battery powered equipment, such as wireless handsets. TI is addressing these issues with advances in both its manufacturing technology and circuit design techniques. For example, as more memory is required on chips for fast execution of software, it occupies an ever increasing part of the SoC, making it an ideal target for new approaches in power reduction. At the VLSI Symposium, TI researchers are describing retention mode bias and other voltage reduction techniques for embedded Static Random Access Memory (SRAM) that greatly reduces the power needed for a memory cell to retain the information it contains. The retention mode bias condition, combined with selective gate cell sizing, can reduce leakage in the transistor by 300X, translating into much lower power consumption across the millions of transistors included on chips with large memories. TI plans to offer extremely dense embedded SRAM with its 65nm process, with the six transistors in a cell occupying less than half a square micron of area and 1.5 Megabits fitting in a square millimeter. An extremely small SRAM cell allows TI to integrate very large amounts of memory close to its processor cores, accelerating application execution.

Earlier this year TI announced it plans to introduce its SmartReflexTM dynamic power management technology at the 65nm node in chips for wireless applications. This innovative technology will automatically scale power supply voltage depending on user demands, thereby helping to control power consumption in devices like TI´s OMAPTM application processors. Using SmartReflex, circuit speed is carefully monitored so that the voltage can be adjusted to exactly meet the performance requirements without sacrificing system performance. As a result, minimum power is used for each operating frequency, extending battery life and reducing the amount of heat produced by the device. The 65nm process featured in the low power paper presented this week has been

optimized to support the SmartReflex dynamic power management technology.

Innovative Strained Silicon Approach

To continue improvements in transistor performance for its microprocessor-class products, TI is pursuing strained silicon as a way to increase drive current, a primary factor in transistor switching speed, which in turn determines processor operating speed. The semiconductor industry has explored a number of different techniques to increase current flow by introducing regions enriched with germanium atoms to strain the silicon and make it easier for electrons to move. Competitors have announced processes that use various levels of silicon germanium (SiGe) to achieve a strain, in some cases using SiGe across the entire wafer. SiGe can introduce unwanted defects and the more of the material introduced, the more yield-killing defects are seen. TI believes it is using the smallest amount of SiGe in the industry and placing it much closer to the transistor channel than previously demonstrated to achieve the maximum strain with the fewest defects. Combined with an industry leading, 37nm gate length and highly effective gate dielectric scaling, TI is showing a 35 percent drive current improvement at the VLSI Symposium.

The original press release can be found here.