Silterra and IMEC Join for 0.13-micron CMOS Process Technology

June 29 2004

Silterra Malaysia Sdn. Bhd., and IMEC, Europe's leading independent nanoelectronics and nanotechnology research center based in Belgium, today announced that they have signed an agreement for a joint development project (JDP) with the intention of creating a foundry-compatible 0.13-micron CMOS process technology. The process will be based on IMEC's 0.13-micron platform technology and modified to meet the requirements of wafer foundry customers.

"We are excited about this project because IMEC is well known for its world-class R&D expertise," said Bruce Gray, executive vice president and chief operating officer of Silterra. "We have already completed the groundwork with customers to define their technology requirements and understand their specifications. Together Silterra and IMEC will take the next steps to develop a compatible 0.13-micron technology for the foundry industry."

A team of Silterra and IMEC engineers will fine-tune the base-IMEC process at IMEC's research facility in Leuven to meet the specifications provided by Silterra. The process will have physical design rules and electrical characteristics that match mainstream technologies, enabling customers to seamlessly support their multi-foundry sourcing strategy. The technology will have FSG (fluoro-silicate glass) or low-K inter-metal dielectric options and up to eight layers of copper interconnect.

"The wafer foundry business is an important part of the semiconductor supply chain," stated Prof. Gilbert Declerck, president and CEO of

IMEC. "We are very happy to partner with Silterra to develop a technology that will benefit such a wide customer base. Our 0.13-micron platform technology is a great starting point to build on because it is proven and will help shorten development cycle times significantly."

The new process, like Silterra's own foundry compatible 0.18- and 0.22-micron logic technologies, is targeted for a wide range of products for communications, consumer and computational applications. Silterra expects to provide supporting design libraries and IP in Q1 2005, with pilot production starting in Q2 2005.

The original press release can be found here.