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Samsung Electronics Develops Wafer Level Package for High-Performance SDRAM

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Samsung Electronics Co., Ltd., the world leader in advanced semiconductor memory technology, announced the industry's first wafer level package (WLP) for high-performance 512Megabit (Mb) DDR2 SDRAMs. WLP, unlike conventional package technology, builds the package layer directly on the wafer by incorporating fabrication process. This new approach enhances the electrical properties and reduces the physical space making WLP an optimal package solution for mobile environments and high-density memory modules.

The new package technology, WLC, is originated from the wafer level process. Two patterned inter-layer dielectrics (ILD), with insulating characteristics, and a metal layer replaces the conventional package substrate. Ball grids give the appearance of a chip scale package (CSP) that is truly scaled down to the actual die size.

The compact new package enhances electrical properties though shorter circuit-routing, reduces package size to die level and package process time, and brings higher productivity, especially to larger wafer sizes, with higher throughput and lower cost. The WLP also enhances environment protection measures as eliminating the conventional package removes need to acquire and treat the package or its remains making WLP a competitive choice over conventional packages.

Samsung's WLP supports the JEDEC specifications for DDR2 CSP. Without further modification the DDR2 WLP can easily replace the CSP form allowing system designers to facilitate the introduction of

WLP for DDR2 SDRAM applications.

Original press release at: www.samsung.com/

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