NEC announced multi- level Cu/Low-k interconnects for second generation 65nm-node VLSIs

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NEC Corporation and NEC Electronics Corporation announced that they have succeeded in the development of multi- level Cu/Low-k interconnects for second generation 65nm-node VLSIs. By improving the interconnect structure and dielectric material, reduction of the effective dielectric constant, keff, to the target value of keff equals 3.0 was successfully demonstrated, without degrading reliability. In addition, interconnect power consumption was reduced by 15%, and signal speed was improved by 24%, as compared with conventional structures.

The features of the newly developed Cu/Low-k interconnect are as follows:
(1) Development of high performance multi-level interconnects with Dual Damascene (DD) structure for second generation 65nm node, low-power VLSIs.
(2) Development of DD interconnect structures introducing the porous low-k dielectrics with sub-nanometer pores, both for line dielectrics and via dielectrics, and interconnect parasitic capacitance, which achieved an interconnect power consumption reduction of 15%. Through the coupling of the thin barrier metal with the DD structure, the interconnect CR product boasted a 24% improvement in interconnect performance (as compared with conventional products).
(3) Development of a "DD pore sealing technique", which entails the covering of all the side walls of porous low-k films with an ultra-thin organic low-k film, enabled an improvement in dielectric reliability by 5

times.

In advanced SOCs, the number of lines and the total line length tend to increase by the device scaling-rule, resulting in a rapid increase in the ratio of interconnect load capacitance against the total chip load capacitance. Thus, in order to reduce chip power consumption, the introduction of low-k materials into interconnects is an inevitable requirement. We have adopted a dual damascene (DD) structure in which the line trench and the via hole are simultaneously filled with copper. Compared with the single damascene structure, where the line and via are formed independently, the parasitic capacitance of the DD structure was reduced by 10% due to a decrease in the number of capping dielectrics with relatively high k-value. In addition, through the introduction of a porous low-k film for both via and line dielectrics, a further reduction of 5 % was achieved.

Key fabrication technologies for high performance DD interconnects with porous low-k films are as follows:
1) An etching technique which can reduce plasma damage to low-k films.
2) A low thermal budget process that can suppress thermal stress on Cu interconnects.

How to secure via dielectric reliability is a critical issue for introducing the porous low-k film to the via dielectric. In order to secure via dielectric reliability, we developed a DD pore sealing technique. Plasma polymerized BCB (p-BCB) film, developed by NEC, was used as pore sealing film. In addition, since the p-BCB film has strong resistance to the Cu diffusion as well as relatively low k-value, the barrier metal can be extensively thinned. Consequently, using the DD pore sealing technique, the line resistance and the via resistance were reduced by 9% and 75%, respectively.

NEC Corporation believes that such newly developed technologies for multi level interconnect modules with porous low-k films are needed for 65nm node low power LSIs and will make every effort to realize their early production. NEC Corporation will present these results at the 2004 Symposia on VLSI Technology in Hawaii, USA, on June 15, 2004.

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