International SEMATECH Identifies Top Technical Challenges for 2005

June 14 2004

International SEMATECH released its Top Technical Challenges for 2005, re-emphasizing advanced gate stack, 193nm immersion and EUV lithography, and low-k dielectrics, and placing 3-D interconnect on the list for the first time.

SEMATECH uses the Top Challenges list to focus resources on the most critical of approximately 90 projects that it maintains in key areas of semiconductor R&D. The SEMATECH research portfolio is developed by the consortium's Executive Steering Council (ESC), in consultation with corporate managers.

"This list of challenges reflects our members' view of where we can best utilize our key skills and resources for the benefit of both the SEMATECH membership and the industry," said Dr. Michael R. Polcari, SEMATECH president and CEO.

"Each of these challenges corresponds to critical infrastructure needs in lithography, advanced materials, and manufacturing, as identified in the International Technology Roadmap for Semiconductors (ITRS). SEMATECH's role is to help drive the advanced technology and manufacturing breakthroughs that lay the foundation for emerging technologies," he added.

The SEMATECH challenges reflect member consensus, and include:

Lithography

- Immersion Lithography, a new approach for optical patterning that interposes a liquid between an exposure tool's projection lens and a wafer to achieve better depth of focus and resolution over conventional projection lithography. Recent industry symposia hosted by SEMATECH showed 193 nm immersion to be a viable technology for rapid introduction into manufacturing.
- Mask Infrastructure, including attention to improving the capabilities and reducing the overall cost of photomasks. SEMATECH remains committed to finding innovative and cost-effective mask solutions to ensure the affordable evolution of lithography.
- Resist Strategy, a high-priority response to the requirements of new and emerging litho technologies, including 193 nm immersion and extreme ultraviolet (EUV). Line edge roughness (LER) and limits of chemically amplified resists (CARs) are among within the strategy's focus.
- EUV Infrastructure, which includes the testing and development of masks, tool components, and resists to enable the introduction of extreme ultraviolet lithography into manufacturing later in the decade.

Front End Processes

- Advanced Gate Stack, involving development of new gate stack materials and processes, primarily manufacturing readiness of hafnium-based, high-k dielectrics and metal gate electrodes.
- Non-classical CMOS, an approach to the challenges posed by increased scaling of chip features. Non-classical CMOS includes infrastructure development (such as metrology techniques) for alternative device technologies, such as strained silicon, silicon-on-insulator (SOI) and double-gate metal-oxide semiconductor field-effect transistors (MOSFETs).

Interconnect

- Low-k Dielectrics and Process Compatibility. Low-k is critical to advanced semiconductor manufacturing because it allows metal lines to be packed closer together on a chip with less risk of electrical signal leakage. SEMATECH engineers investigate low-k materials and assist layers necessary for successful integration and achievement of low k-effective values. The program includes extensive work in advanced barrier development, and work on understanding and finding solutions for ultra fine line Cu resistivity increases seen at the 32 nm and 22 nm nodes.
- 3D Interconnect Technology, which seeks to provide an alternative to conventional scaling of complementary metal-oxide semiconductor (CMOS) structures by physically interconnecting several chips to produce similar speed and density. In early April, SEMATECH kicked off this effort by cosponsoring a technical symposium and industry workshop in 3-D interconnect challenges and architecture in Burlingame, CA.

Manufacturing

- Metrology, a critical enabler to the achievement of increasing device densities and decreasing feature sizes on advanced semiconductors.
- Manufacturing Effectiveness and Productivity, involving an array of fab-related projects including improved equipment productivity; e-manufacturing; advanced equipment and process control; and standards development.
- Environment, Safety and Health, as a cross-cut priority for each of the Top Challenges, addressing ESH considerations related to the introduction of new materials and process chemicals into advanced manufacturing.

"These challenges demand innovative solutions," said Polcari. "SEMATECH is uniquely positioned to deliver to its members high-value, high-leverage programs in each of these areas, and to help lead the industry in realizing the Roadmap."

The original press release can be found here.

Citation: International SEMATECH Identifies Top Technical Challenges for 2005 (2004, June 14) retrieved 23 April 2024 from https://phys.org/news/2004-06-international-sematech-technical.html

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