IBM Introduces Advanced Design Methodology to Increase Performance and Reduce Power Consumption in Custom Chips

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SAN DIEGO, CA -- Jun 9, 2004 -- IBM today introduced an **industry-first timing flow created to maximize performance and minimize power consumption in next-generation custom chips**.

Called 'variation-aware timing', this revolutionary methodology is expected to reduce custom chip design turnaround time by as much as 4X and help to further enable designs that are completed right the first time, meaning faster time-to-market for customers. The methodology is targeted at application specific integrated circuit (ASIC) 130nm (nanometer), 90nm and 65nm chip designs.

"In order to maintain our ASIC leadership, we intend to stay ahead of the innovation curve," said Richard Busch, director of ASIC business development, IBM Systems & Technology Group. "IBM's start-to-finish design solutions seamlessly integrate proven methodologies, tools and services to assure customers fast time to market at a competitive edge. We will continue to invest in leadership tools and methodologies to address the design challenges facing next-generation devices."

As chips become increasingly complex and the industry evolves into using smaller and smaller geometries, there are more variables that could affect the integrity of the design. A slight error can become magnified as dimensions shrink. Not only are the chips smaller, but this closer

proximity of devices and wiring causes formerly small variations to now translate into a significant percentage of the electrical signal being transmitted. Factors such as threshold voltages, line width and gate width, all subject to process variation, now significantly impact chip design and performance and must be accounted for in the design methodology.

Using variation-aware timing, IBM engineers are now able to account for the different variables in custom chip design by closely analyzing the time it takes electronic signals to pass from circuit to circuit. With the methodology in place, designers are able to correct errors that might previously have gone undetected, enabling them to maximize performance and minimize power consumption, and ultimately build a more robust chip right the first time.

IBM is able to account for these process and environmental variations in real-time and engineer the chip accordingly throughout the design flow, from development through the manufacturing process.

Variation-aware timing is available now as part of the IBM Cu-11 (130nm) and Cu-08 (90nm) ASIC design kits.

The original press release can be found here.