Combination of SRAM and DRAM Capacitor Technology Enables Error-Free Low-Power-Consumption SRAM

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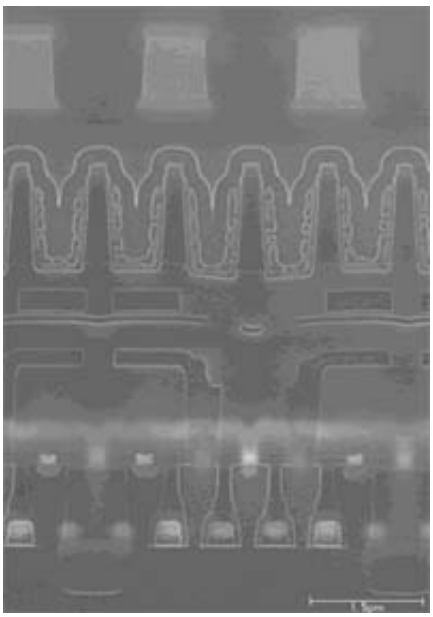

Renesas Technology Corp. has developed the industry's first SRAM virtually free of soft errors, dubbed "superSRAM", through the development a new type of memory cell combining an SRAM cell with a DRAM capacitor technology. This new SRAM will be applied to, and put into commercial production for, the 16M-bit low-power SRAM for mobile applications. Details will be announced at the 2004 Symposium on VLSI Technology to be held in Hawaii in the United States on June

17 (local time).

Normal SRAM cells comprise six transistors: two CMOS type load MOS transistors, two access MOS transistors, and two driver MOS transistors. In the new superSRAM, the two load MOS transistors are replaced by two TFTs located above the access MOS/driver MOS transistors, and two cylindrical capacitors are stacked on top of the node. This design achieves the industry's smallest memory cell size of 0.98 μm2 for 0.15 μm process SRAM. A sub-1 μm2 cell size, considered to be attainable with 90 nm process nodes, has been realized, and the cell size has been reduced to less than half that of conventional Renesas Technology's 0.15 μm process CMOS type SRAM.
Also, the use of DRAM cylindrical capacitors at the storage nodes has enabled capacitance to be increased compared with normal CMOS type RAM, and provides a structure in which soft errors cannot in effect occur, making it possible to provide highly reliable memory devices.

As with conventional SRAM, information stored in a memory cell is automatically maintained by means of the load transistors and driver transistors, so that there is, of course, no need for refreshing. It makes possible an approximately double-digit improvement in data retention current compared with pseudo-SRAM.

The newly developed superSRAM technology fundamentally solves the problem of soft error tolerance associated with finer SRAM processes. It has opened the way to the implementation of a highly reliable large-capacity SRAM. Following on from the 16M model, there are plans for commercial development of 32M-bit superSRAM during the current fiscal year.

The main features of the technology and product are summarized below.

(1) High soft error tolerance

An approximately 4-digit improvement in the soft error rate compared with Renesas Technology's previous 0.13 µm process 16M-bit low-power SRAM (without ECC circuitry) has been achieved by providing a cylindrical capacitor, like the type used for DRAM cells, at each memory cell storage node. Alpha ray radiation experiments have confirmed for the first time that the SRAM performance is free of bit defects due to soft errors.
The problem of soft error tolerance, which is a fundamental issue for conventional SRAM, has been solved, enabling highly reliable, high-density SRAM to be realized.

(2) Industry's smallest memory cell size for a 0.15 µm process SRAM
The development of a new type of cell that combines an SRAM cell using TFTs and a DRAM capacitor has resulted in the industry's smallest memory cell size for a 0.15 µm process SRAM: 0.98 µm2. The cell size is less than half that of Renesas Technology's current CMOS-based 0.15 µm process SRAM. It will enable chip size to be greatly reduced and mobile devices to be made smaller.
In addition, a data retention current of less than 1 µA has been achieved. Unlike a pseudo-SRAM that employs DRAM memory cells, the new SRAM cell does not need refresh operations. That allows an approximately double-digit improvement in data retention current compared with a pseudo-SRAM, for lower power consumption in mobile applications.

(3) Fabrication possible using existing 0.15 µm process
Higher performance and a smaller cell area have been achieved without using special processes. Fabrication is possible using existing process technologies, enabling early introduction to the market.

More information at: www.renesas.com/