Cadence and CoWare Deliver Electronic System-Level (ESL) Design-for-Verification Flow

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System-Level Design Knowledge Reduces Verification Effort by Up to 50%

San Jose, CA , June 1, 2004 -- Cadence Design Systems, Inc. and CoWare(R) Inc., the leading supplier of system-level electronic design automation (EDA) software and services, announced the availability of an integrated, seamless flow from electronic system-level (ESL) design through verification for complex system-on-chip (SoC) designs. The ESL design-for-verification solution-which marks a major milestone on the strategic alliance roadmap between the companies-enables customers to capture system-level design knowledge and apply it later in the design process to reduce verification time by up to 50%. The flow is based on new integration between the latest releases of CoWare's SystemC-based ConvergenSC(TM) SoC design tools and ConvergenSC Model Library and the Cadence(R) Incisive(TM) functional verification platform.

"Providing SystemC models of ARM® IP to enable ESL design is an important step in simplifying the complex SoC design task," said Duncan Bryan, EDA Relations manager, ARM. "The joint flow of CoWare's ConvergenSC tools and Cadence's Incisive platform will enable ARM core-based chip designers to efficiently carry the same SystemC model, software and tests from the system-level design through to chip-level verification. This verification scaling is important to ARM and we welcome these types of alliances."

"We are pleased to announce this milestone in our ongoing strategic relationship with CoWare," said Mitch Weaver, general manager, Systems and Functional Verification Division, Cadence. "Through this combined flow, we are providing customers with consistency and assurance within the development environment from system through silicon, greatly reducing risk and time-to-market. Customers will be able to build systems with verified, reusable hardware and software IP blocks faster and with greater confidence that the systems will be right the first time."

"The increasing size and complexity of designs is creating an enormous opportunity for ESL to impact verification methods," said Mark Milligan, vice president of marketing, CoWare. "Working together, Cadence and CoWare are applying ESL to eliminate major verification challenges, especially for designs with embedded software."

Verification Challenges Addressed by ESL

Today, verification engineers must regenerate system-level test cases that attempt to capture system behavior often known only to the system architect. This is causing an explosion in the resources needed to verify complex SoCs. At the same time, system architects are using high-level models to explore the design space, but verification engineers are unable to reuse those models for RTL verification. This risks a loss of design intent and lack of insight into potentially fatal design flaws.

Embedded software developers are facing similar challenges. To debug their embedded software, developers must often wait for prototypes, which arrive too late in the design process. Alternative RTL co-verification techniques are too slow, and also present challenges for the software developer who may not understand the unverified RTL.

The Cadence/CoWare ESL Design-for-Verification Flow

With the unified flow, system architects can rapidly explore the design

space in ConvergenSC and determine the optimal system architecture for the SoC. Using SystemC transaction level models (TLM), which can deliver simulation speed greater than 10,000 times faster than RTL, the architecture is evaluated using realistic system scenarios with software. These models also provide the accuracy needed for system analysis and optimization. The SystemC model and ConvergenSC software analysis is used by software developers to validate and optimize embedded software early in the design process.

Once validated, the SystemC model becomes a functional virtual prototype (FVP) with an embedded software testbench. Verification engineers use ConvergenSC technology to rapidly reconfigure the FVP as a heterogeneous model. This heterogeneous model in the Incisive platform allows the verification engineer to re-use the knowledge captured in the system to verify the RTL at over 100 times the simulation performance of an all RTL system.

How It Works

ConvergenSC and the Incisive platform include new capabilities to enable the joint flow:

- ConvergenSC and the Incisive platform now share SystemC simulation technology and compiler support, providing for SystemC model interoperability. This means that user SystemC models created in ConvergenSC run identically in Incisive functional verification technology without the need to recompile.
- The world's largest SystemC model library is now available to use with Incisive platform technologies for verification. The ConvergenSC Model Library of SystemC processor support packages (PSPs) and bus libraries simulate in both ConvergenSC and the Incisive platform.
- ConvergenSC also provides a graphical platform-based design environment with automated TLM-to-RTL transactor generation for rapid reconfiguration of mixed SystemC/HDL "FVPs" using the ConvergenSC Model Library and user RTL, and export of the

SystemC/HDL "FVP" netlist to ConvergenSC and the Incisive platform. - Powerful SystemC debugging capabilities in ConvergenSC and Incisive technologies are tailored for system-level modeling and verification. ConvergenSC support for SystemC threads, Incisive unified source-level (SystemC, Verilog, VHDL, etc) debugging environment, and integration with third-party software debuggers result in the most complete environment for SoC verification.

Availability

Cadence Incisive 5.3 and CoWare ConvergenSC 2004.1 are available now worldwide. For pricing information on Cadence products, contact your local sales office or go to www.cadence.com/products/reque … uestproductinfo.aspx. For pricing information on CoWare products, contact your local sales office or email sales@coware.com. For more information, visit www.coware.com.

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