

UMC Announces a Device Technique that Enhances Silicon-on-Insulator (SOI) Transistor Performance

May 26 2004

HSINCHU, Taiwan, May 26, 2004 -- UMC, a world leading semiconductor foundry, today announced the discovery of a **new engineering technique that enhances Silicon-on-Insulator (SOI) transistor performance**. The Direct-Tunneling induced Floating-Body Potential, which is a manipulation technique that magnifies a certain device physics behavior, provides PMOS transistors a 30 percent increase in drive current compared to conventional body-grounded SOI transistors. Unlike other performance enhancing techniques such as strained silicon devices or multi-gate transistors, this new technique suffers no additional process complexity, which translates into a better position in terms of manufacturing cost and yield.

"To further increase our competitiveness, UMC has always researched a variety of possible enabling technologies simultaneously," said S. C. Chien, senior director of UMC's Central Research and Development. "Our discovery on Direct-Tunneling induced Floating-Body Potential for Silicon-on-Insulator transistors not only provides the performance enhancement needed for UMC's future technologies, but also retains good manufacturability, which is a crucial element for a successful semiconductor foundry."

Direct Tunneling is a quantum mechanical behavior where electrons or holes jump through a thin insulator. This usually undesirable behavior can be manipulated with simple design layout structures. SOI devices

could take advantage of this behavior to circumvent the Floating-Body Effect, an uncontrollable parasitic effect. With this extra control, the transistor behaves much more predictably in addition to the performance gain.

A series of publications discussing this technique have been published in the April and May editions of IEEE Electron Device Letters and IEEE Transactions on Electron Devices.

About Silicon-on-Insulator (SOI)

Silicon-on-Insulator is an approach in which transistors are built on top of an insulating material instead of the conventional silicon crystal substrate. By replacing the silicon substrate with an insulator substrate, extra capacitive load produced at the interface between the substrate and the transistor active areas is eliminated. In effect, SOI transistors can switch faster with lower power consumption, compared to conventional bulk silicon transistors. However, the body of the transistor is now sitting on an insulator and therefore electrically isolated from the rest of the circuit. The isolated body leads to the *floating body effect*, which creates an uncontrollable mode that makes transistors behave erratically in certain circumstances.

Full press-release on www.umc.com

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