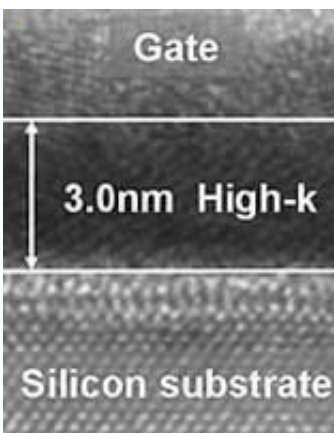


Intel's Breakthrough in High-K Gate Dielectric Drives Moore's Law Well into the Future

May 12 2004



After several years of effort, the Intel technology team has made a major breakthrough that solves the chip power problem. Intel has identified a new material known as "high-K" to replace SiO₂ as the gate dielectric, in addition to new metals to replace the polysilicon gate electrode of NMOS and PMOS transistors.

These new materials, when implemented with the correct process recipe, reduce gate leakage by over 100-fold, while delivering record transistor performance. Intel is on track to implement this new technology in the 45 nm node in 2007. The breakthrough will drive Moore's Law into the next decade.

In a groundbreaking article written in 1965, Gordon Moore described exponential growth in the number of transistors per integrated circuit and predicted this trend would continue. "Moore's Law," states that the number of transistors on integrated circuits doubles approximately every 24 months, resulting in higher performance at lower cost.

This simple but profound statement is the foundation of semiconductor and computing industries. It is the basis for the exponential growth of computing power, component integration that has stimulated the emergence of generation after generation of PCs and intelligent devices.

Perhaps the most vital question for the industry is: how much longer can Moore's Law continue?

As transistor geometries scale to the point where the traditional silicon dioxide (SiO_2) gate dielectric becomes just a few atomic layers thick, tunneling current leakage and the resulting increase in power dissipation and heat become critical issues. The mission of Intel's technology development team in Components Research is to break down the barriers and keep Moore's Law rolling forward. Solving the gate dielectric problem is a critical issue for the industry.

After several years of intensive effort the Intel research team has identified a new material known as "high-K" to replace SiO_2 as the gate dielectric. To resolve compatibility issues with this new high-K dielectric, Intel also needed to discover new metals to replace the traditional polysilicon gate electrode used in NMOS (negative polarity metal oxide semiconductor) and PMOS (positive polarity metal oxide semiconductors) transistors.

For three decades, SiO_2 formed the perfect gate dielectric material, successfully scaling from a thickness of 1,000 Å (100 nm) 30 years ago to a mere 12 Å (1.2 nm) at today's 90 nm process node. This represents a

layer only five atoms thick.

The problem is that as the oxide layer gets thinner, the rate of gate leakage tunneling goes up. Current leakage contributes to power dissipation and heat.

After five years of research, Intel has found the right high-k material and has identified the right type of gate electrode materials for both NMOS and PMOS technologies, while at the same time achieving record performance. By moving to a new high-k material, Intel was able to keep the drive current at the level it could have achieved in older materials — and overcome the leakage.

"This is the first convincing demonstration that new gate materials will enable transistors to perform better, while overcoming the fundamental limits of the silicon dioxide gate dielectric material that has served the industry for more than three decades," says Sunlin Chou, Intel senior vice president and general manager of the Technology and Manufacturing Group. "Intel will use this advancement along with other innovations, such as strained silicon and tri-gate transistors, to extend transistor scaling and Moore's Law."

Of course, Intel does not disclose the high-k material they used saying only that "most of the high-K gate dielectrics investigated are Hf-based and Zr-based".

Find more details on [Intel web-site](#).

Citation: Intel's Breakthrough in High-K Gate Dielectric Drives Moore's Law Well into the Future (2004, May 12) retrieved 20 March 2024 from <https://phys.org/news/2004-05-intel-breakthrough-high-k-gate-dielectric.html>

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