IMEC presents novel non-volatile memory capable of storing 9 bits per cell

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IMEC (Leuven, Belgium) has developed a novel non-volatile memory cell, based on a dual-gate transistor with an oxide-nitride-oxide charge-trapping dielectric underneath the drain-side gate, capable of storing 9 bits per cell. Details of the device are to be presented at the 2004 Symposia on VLSI Technology and Circuits.

Researchers from IMEC have developed a device they call a "ScanROM" that can store 9-bits per memory cell. Multiple bits are stored along the width of the device. By contacting the gates from both sides and applying an appropriate bias difference to each, the individual bits are addressed. Authors say that they experimentally demonstrated reading and writing of 9-bits in a prototype cell.

Up till now, Saifun Semiconductor Ltd. (Netanya, Israel) has demonstrated the ability to store two bits within one cell. This is done by

using two distinct charge areas at each end of a flash memory floating gate. This technology is used in Spansion memory products that are now offered by AMD and Fujitsu.

Saifun said it has been working for several years on the 4-bit-per-cell technology by combining two storage sites with two voltage levels per memory cell.

See more:
www.imec.be/
www.amd.com