High-K Progress Towards 45 nm

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STMicroelectronics, CEA-Leti and AIXTRON Develop Ultra-Thin Gate-Insulation Process for Advanced CMOS Transistors

Geneva, May 26, 2004 - STMicroelectronics today announced that ST, CEA-Leti and AIXTRON have developed an advanced process technology for the creation of ultra-thin transistor-gate-insulation layers for low-power applications at the 65nm and 45nm CMOS transistor technology nodes. The new process significantly reduces transistor leakage current by the deposition of 'high-k' gate-insulation material.

To meet the future requirements of highly integrated devices postulated by Moore's law and described via the International Technology Roadmap for Semiconductors (ITRS), it will eventually be necessary to introduce new materials into the manufacture of advanced silicon devices. The three companies are developing new process technology aimed at the 45nm or 65nm technology nodes for low-power CMOS platforms optimized for portable applications.

Based on AIXTRON's Tricent® reactor technology, CEA-Leti and ST have created a joint development program for 'high-k' materials, fulfilling the specifications of advanced nano-metric CMOS gate-stacks that require a thick physical layer with a low leakage current equivalent to ultra-thin oxide.

The process, called AVD® (Atomic Vapor Deposition), has demonstrated excellent Equivalent Oxide Thickness (EOT) values of 1.15nm or 11.5Å (Angstroms) based on hafnium dioxide / silicon

dioxide / silicon (HfO2/SiO2/Si) stacks offering leakage current densities as low as JL=6.8·10-2A/cm2 at 1.5V.

The results were obtained by the Advanced Modules team of researchers from ST and CEA-Leti at ST's Crolles facility using a Tricent AIXTRON 200/300 mm bridge cluster tool. The HfO2 deposited layer process was developed in conjunction with AIXTRON, and the wafer processing and the characterization were performed at CEA-LETI facilities in Grenoble.

Metallic oxides of the hafnium family are believed to be excellent candidates for the 'high-k' dielectric material that will eventually replace silicon dioxide in the basic CMOS transistor structure.

In addition to the ability to precisely deposit thin dielectric 'high-k' layers, the AVD technique also allows the deposition of metal gates necessary for the 45nm-and-below CMOS technology nodes.

"These proof-of-concept results are a first for this process technology," said Daniel Bensahel, Project Leader and Front-End Program Director at STMicroelectronics. "This joint development program between ST and CEA-Leti, in conjunction with AIXTRON, is not only the first in the industry to implement this advanced process in an industrial environment; but more importantly, it is also achieving excellent results."

"The co-operation with STMicroelectronics and CEA-Leti is an integral part of our strategic CMOS development effort strengthening AIXTRON's position in emerging semiconductor applications. By working with one of the leading semiconductor device manufacturers and one of the top research organizations in the industry, AIXTRON will remain at the forefront of cutting edge enabling MOCVD process technology development. We have been highly impressed by the professionalism and the technical competencies of the

STMicroelectronics and CEA-Leti team, and look forward to combining our expertise to develop solutions for advanced CMOS devices," said Tim McEntee, Executive Vice President and COO Semiconductor Equipment/ AIXTRON AG.

Find the original press release here.