Cadence Delivers 90-Nanometer Reference Flow to Optimize Nanometer Design for IBM-Chartered Process Platform

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Cadence Encounter-Based Reference Flow to Provide High Quality of Silicon for Complex 90-Nanometer System-on-Chip Designs

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Cadence Design Systems, Inc. (NYSE:CDN) today announced the availability of a qualified design reference flow validated as compatible with the IBM-Chartered 90-nanometer process platform. The Cadence reference flow seamlessly integrates intellectual property (IP) developed by Artisan Components, Inc. for the IBM-Chartered cross-foundry design enablement program. Developed in conjunction with IBM, this RTL-to-GDSII reference flow—based on the Cadence Encounter digital IC design platform—is optimized across the front-to-back design chain. It offers chip designers a predictable path for system-on-chip (SoC) design from RTL to first-pass silicon.

The reference flow incorporates leading Cadence technologies including Encounter RTL Compiler™ global synthesis, Encounter Test™ solutions, and NanoRoute™ unified routing and physical optimization.

"This reference flow is another significant step in the ongoing collaboration between Cadence and IBM. Cadence, Chartered and IBM customers will be able to use this reference flow to optimize their design process," said Tom Reeves, vice president, semiconductor products and

solutions, IBM Systems & Technology Group. "It will enable a faster path to volume silicon using the leading-edge IBM-Chartered 90-nanometer CMOS process technologies."

The joint reference flow uses a wire-centric methodology to address key 90-nanometer SoC issues, including low power design, signal integrity, and design-for-test to provide the highest quality of silicon (QoS). QoS measures a design's physical characteristics using wires in terms of improved area utilization, higher performance and lower power consumption.

"The combination of advanced process technology, jointly developed by IBM, Chartered and leading-edge Cadence technologies, allows customers to benefit from improved quality of silicon resulting in reduced area, lower power and better performance," said Lavi Lev, executive vice president and general manager, IC Solutions, Cadence. "Ultimately, our goal is to provide mutual customers with a predictable path to first silicon."

"The Cadence Encounter platform focuses on some of the more challenging issues with regard to 90-nanometer design, and we're pleased to be collaborating with Cadence as a means for customers to accelerate their path to silicon," said Kevin Meyer, vice president of worldwide marketing and services at Chartered. "By leveraging the IBM-Chartered design enablement program, customers enjoy additional benefits such as design portability and a flexible sourcing model."

The original press release can be found here.

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